Name of the Faculty	**Dr. Md. Salauddin**		
Designation	Associate Professor of ECE & Dean Academics		
Date of Joining	19-06-2018		
E - Mail	deanacademics@jbiet.edu.in; salal.vlsi@gmail.com		
Educational Qualifications	**Name of the Degree**	**Institute**	**Class**
Ph. D	Doctor of Philosophy (Electronics Engineering)	UPES, Dehradun	Awarded
PG	M. Tech (VLSI System Design)	SKEC, Khammam	First
UG	B.Tech (Electronics and Communication Engineering)	SKEC, Khammam	First
Work Experience			
Teaching	16 Years		
Research	5 Years		
Industry	-		
Responsibilities held at the central level in college	• Dean Academics (12-07-2021 to till now) • Chief Coordinator for AICTE Margdarshan Scheme • Dean Quality Control • NBA Coordinator • HOD-ECE • Member Secretary, Academic Council • Member, Board of Governors		
Responsibilities held at the departmental level in college	• Head of the Department from 26-06-2018 to 03-05-2019. • Chairman, Board of Studies from 26-06-2018 to 03-05-2019.		
Courses Handled at UG Level	• Digital System Design Course for B. Tech Second Year Students. • Probability Theory and Stochastic Process Course for B. Tech Second Year Students. • VLSI Design Course for B. Tech Third Year Students. • Embedded Systems Course for B. Tech Third Year Students.		
Courses Handled at PG Level	• Advanced Digital System Design for M. Tech VLSI System Design First Year Students. • CAD for VLSI for M. Tech VLSI System Design Second Year Students. • DSD using HDL for M. Tech VLSI System Design First Year Students. • Low Power VLSI Design for M. Tech VLSI System Design Second Year Students.		

Area of Research	• VLSI System Design using FPGAs. • Certified in FPGA-based VHDL Design for Advanced Mobile Algorithms & Architectures.
Research Guidance for M. Tech/ Ph. D Students	• Design and Implementation of a High-Performance FIR Filter using VLSI • FPGA-based Real-Time Face Recognition System • Low Power VLSI Design Techniques for IoT Applications • Implementation of AES Encryption Algorithm on FPGA • Design of Low Power CMOS Image Sensor • VLSI Design of Energy-Efficient Neural Network Accelerator • FPGA-based Hardware Acceleration for Deep Learning Applications • Design and Optimization of Low Power Adder Circuits • VLSI Implementation of Digital Signal Processing Algorithms • FPGA-based Hardware Security Module for Cryptography • Energy-Efficient VLSI Design for Wireless Sensor Networks • Design and Implementation of a Reconfigurable Computing System on FPGA • Low Power VLSI Architecture for Convolutional Neural Networks • FPGA-based Real-Time Video Processing System • Hardware Implementation of Error Correction Codes for Memory Systems • VLSI Design of High-Speed Serial Communication Interfaces • Design and Optimization of Power Gating Techniques in VLSI Circuits • FPGA-based Implementation of a Traffic Light Controller • Low Power VLSI Design for Biomedical Signal Processing • Design of High-Speed Data Converters using VLSI • Implementation of FIR Filter Bank for Audio Processing on FPGA • Energy-Efficient VLSI Design for Internet of Things (IoT) Nodes • FPGA-based Acceleration of Computer Vision Algorithms • Design and Optimization of Low Power Clock Distribution Networks • VLSI Implementation of Reconfigurable Digital Filters • FPGA-based Hardware Acceleration for Machine Learning Algorithms
Books/ Book Chapters Published	• Book: Digital Forensics and Internet of Things in Xilinx FPGA and Xilinx IP Cores: A Boon to Curb Digital Crime, Scrivener Publishing, Wiley Chapter 9, Pg: 178-198, 2022 • Implementation of FM based Communication system with 3-Level parallel multiplier Structure for Fast Transmission using FPGA in Intelligent Communication, Control and Devices; Advances in Intelligent Systems and Computing, vol 989. Springer, Singapore. https://doi.org/10.1007/978- 981-13-8618-3_64, 2019 • Detection of DTMF By Using Goertzal Algorithm And optimized resource Sharing Approach in Intelligent Communication, Control and Devices. Advances in Intelligent Systems and Computing, vol 989. Springer, Singapore. https://doi.org/10.1007/978-981-13-8618- 3_87 • Mitigation of Signal Interference by positioning FFT window for OFDMA system in Intelligent Communication, Control and Devices. Advances in Intelligent Systems and Computing, vol 624. Springer, Singapore. https://doi.org/10.1007/978-981-10-5903- 2_57 • Achievable spectral efficiency with SIT based channel estimation in 4G and 5G cellular networks in Advances in Intelligent Systems and

<table>
<tr><td></td><td>Computing, vol 624. Springer, Singapore. https://doi.org/10.1007/978-981-10-5903- 2_28</td></tr>
<tr><td>Prominent Research Publications in Conferences</td><td>

1Salauddin Mohammad 2, K. Snehalatha 3Durai Pandy 4Towheed sulthana, Design and Implementation of Reconfigurable Polyphase Filter Bank Receiver on Artix-7 FPGA in 2019 IEEE International Conference on Intelligent Techniques in Control, Optimization and Signal Processing (INCOS), 2019, pp. 1-3, doi: 10.1109/INCOS45849.2019.8951338.
1Salauddin Mohammad, 2R. Seetha, 3S. Jayamangala, 4B.Khaleelu Rehman, Implementation of FM based Communication system with 3-Level parallel multiplier Structure for Fast Transmission using FPGA in Intelligent Communication, Control and Devices; Advances in Intelligent Systems and Computing, vol 989. Springer, Singapore. https://doi.org/10.1007/978- 981-13-8618-3_64, 2019
B. Khaleelu Rehman, Adesh Kumar, Salauddin Mohammad, Detection of DTMF By Using Goertzal Algorithm And optimized resource Sharing Approach in Intelligent Communication, Control and Devices. Advances in Intelligent Systems and Computing, vol 989. Springer, Singapore. https://doi.org/10.1007/978-981-13-8618- 3_87
Salauddin Mohammad, Madan Gopal, Rajarao Manda & Khaleel Rehman, Mitigation of Signal Interference by positioning FFT window for OFDMA system in Intelligent Communication, Control and Devices. Advances in Intelligent Systems and Computing, vol 624. Springer, Singapore. https://doi.org/10.1007/978-981-10-5903- 2_57
Rajarao Manda and Mohammad Salauddin, Achievable spectral efficiency with SIT based channel estimation in 4G and 5G cellular networks in Advances in Intelligent Systems and Computing, vol 624. Springer, Singapore. https://doi.org/10.1007/978-981-10-5903- 2_28
Salauddin Mohammad, Dr. Piyush Kuchhal, Dr. Rajeev Gupta, The Digital Tracking Loop Enhancements for Mitigating Signal Interference in DVB-H and DVB-T in International conference on Intelligent Systems, Control and Manufacturing Technology, AbuDhabi ISBN 978-93-84422-10-3

</td></tr>
<tr><td>Prominent Research Publications in Journals</td><td>
<table>
<tr><th>Name of the Author(s)</th><th>Name of the Journal</th><th>Title of the paper</th><th>Index ed in</th><th>Vol. No and Page nos.</th><th>ISBN/ ISSN</th><th>Date</th></tr>
<tr><td>Dr. Towheed Sultana, Mohammad Salauddin</td><td>Taylor and Francis</td><td>Studies on transport and sensing properties of Metal oxide nano composites</td><td>SCI</td><td></td><td>Submission ID: 2389289 5
1</td><td>Publication in Progress</td></tr>
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		Adesh Kumar, Gaurav Verma, Mukul Kumar Gupta, Mohammad Salauddin, B. Khaleelu Rehman & Deepak Kumar	Springer-wireless personal communications	3D Multilayer Mesh NoC Communication and FPGA Synthesis	SCI	106 and Pg: 1855–1873	10.1007/s 11277-018-5724-3	12-04-2018
		B. Khaleelu Rehman1, G. Vallathan1, Vetriveeran Rajamani1 and Salauddin Mohammad2 *	Book: Digital Forensics and Internet of Things	Xilinx FPGA and Xilinx IP Cores: A Boon to Curb Digital Crime	Scrivener Publishing, Wiley	Chapter 9, Pg: 178-198	ISBN 978-1-119-76878-4	2022
		Mohammed moheez 1, MD salauddin 2, K Shilpa 3	Journal of Engineering Sciences	Enhancing Data Integrity In Advanced Space Communications Through LDPC Codes	UGC Care	Vol 15 Issue 1 and Pg: 43 to 56	ISSN:0377-9254	2024
		Gulam Sadeeduddin1 , Koyyada Rakesh2 , Suraiya Shabnam3 , Dr MD Salauddin4	International Journal of System Design and Information Processing (IJSDIP)	FPGA to FPGA Communication With Real Time Serial Data Interface	UGC Care	Volume - 11, Issue-1_Page_131-141	ISSN: (Print): 2319-9288	2023

		Parshi Shruthi1, MD.Salaud di n2	International Journal of Research	Design And Simulation Of FFT/IFFT Blocks For Orthogonal Frequency Division Multiplexing (OFDM) System Using VHDL	UGC Care	Volume XI, Issue XII, Pg: 122-132	ISSN NO:2236 - 6124	Decem ber /2022
		B. Khaleelu Rehman, Ramalla Isaac, K. Abdul Munaf, Salauddin Mohamma d, and Mudassar Basha	Springer	FPGA Implementati on of Area Efficient Binary Counter Using Xilinx IP Cores	Scop u s	Pg: 147 to 156	https:// do i.org/10. 1 007/978 - 981-16- 6647- 6_14	Jan 2022
		K.Krishnam urt hy1, Shaik Shoaib2, Cheguri Vinay Reddy3, MD.Salaud di n4	International Journal of Innovative Research In Technology	Smart Device for Disabled Person	UGC Care	Vol. 9 and pg: 126-130	2349- 6002	June 2022
		A .CHANDA NA PRIYA 1 MD. SALAUDD IN 2 P.SRINIVA SA RAO 3	Journal of Interdisciplin nary Cycle Research	CHIP-SCOPE BASED SPEED OPTIMIZATI ON OF SCALABLE DEEP LEARNING ACCELERAT OR UNIT	UGC Care	Vol 13. And Pg: 1145 to 1151	0022- 1945	Feb-2021

				USING VHDL				
		G. SAI PAVANI1 K. JYOTHI2 K. URMILA3 MD. SALAUDDIN4	Journal of Interdisciplina ry Cycle Research	IOT based garbage monitoring system	UGC Care	Vol.13 and Pg: 1936 to 1940	0022-1945	June-2021
		B. Khaleelu Rehman1. Waaiz Mohammad2. Mudasar Basha3. Salauddin Mohammad4	International Journal of Technology, Management & Knowledge Processing	Hardware Implementation of Parallel adder/Subtarct or and Complex Muliplier using Xilinx IP-Core	UGC Care	Vol 1 and Pg: 6 to 11		Aug-2021
		Rapaka. Sravani 1, MD. Salauddin 2	Journal of Engineering Sciences	Design of single precision floating point multiplier using FPGA	UGC Care	Vol 12 and Pg: 203 to 211	0377-9254	Nov-2021
		Md Salauddin, G Prathyusha	Journal of Interdisciplina ry Cycle Research	An FPGA based Phase Measurement System	UGC Care	Vol.13 and Pg: 338 to 344	0022-1945	Nov-2021

		1Salauddin Mohammad 2, K. Snehalatha 3Durai Pandy 4Towheed sulthana	IEEE Explore	Design and Implementation of Reconfigurable Polyphase Filter Bank Receiver on Artix-7 FPGA	IEEE		10.1109/INCOS458 49.2019. 8951338	09-01-2020
		1Salauddin Mohammad, 2R. Seetha, 3S. Jayamangala, 4B.Khaleelu Rehman	Springer	Implementation of FM based Communication system with 3- Level parallel multiplier Structure for Fast Transmission using FPGA	Scopus	AISC Vol:989 and Pg: 619-626	https://doi.org/10.1007/978-981-13-8618-3_64	Aug-2019
		B. Khaleelu Rehman, Adesh Kumar, Salauddin Mohammad, Mudasar Basha & K. Venkata Siva Reddy	Springer	Detection of DTMF By Using Goertzal Algorithm And optimized resource Sharing Approach	Scopus	AISC, Vol: 989, and Pg: 851-856	https://doi.org/10.1007/978-981-13-8618-3_87	Aug-2019
		S Shruthi, Md Salauddin	International Journal of Research In Electronics And Computer Engineering	Global Enhanced and Consistent Address Methods based on Memory, FFT	UGC Care	Vol:6 and Pg: 1236-1238	2393-9028	Dec-2018

				Processor Design				
		Rajarao Manda and Mohammad Salauddin	Springer	Achievable spectral efficiency with SIT based channel estimation in 4G and 5G cellular networks	Scopus	AISC, volume 624, Pg: 257-265	https://doi.org/10.1007/978-981-10-5903-2_28	2018
		Salauddin Mohammad, Madan Gopal, Rajarao Manda & Khaleel Rehman	Springer	Mitigation of Signal Interference by positioning FFT window for OFDMA system	Scopus	AISC, volume 624, Pg: 561-568	https://doi.org/10.1007/978-981-10-5903-2_57	2018
		Dr. Salauddin Mohammad, Dr. Abhinav Sharma	International Journal of Scientific & Engineering Research	Reduction of BER in the physical Layer of OFDMA	UGC Care	Vol: 8 and Pg: 106-115	2229-5518	Dec-2017
		Dr. Abhinav Sharma, Dr. Salauddin Mohammad	International Journal of Scientific & Engineering Research	Comparative Analysis of Adaptive Beamforming Algorithms for Wireless Communication	UGC Care	Vol: 8 and Pg: 122-130	2229-5518	Dec-2017

		Salauddin Mohammad1, Piyush Kuchhal2 and Rajeev Kumar Gupta3	International Journal of Applied Engineering Research	BER Performance of OFDM System with various OFDM frames in AWGN, Rayleigh and Rician Fading Channel	Scopus	Volume 10, pg: 39911-39916	0973-4562	2015
		Salauddin Mohammad1, Piyush Kuchhal2 and Rajeev Kumar Gupta3 •	International Journal of Applied Engineering Research	FPGA Design and Implementation of FFT processor for OFDMA system	Scopus	Volume 10, pg: 43923-43925	0973-4562	2015
Web of Science/**Scopus ID**		KBD-1144-2024						
Google Scholar ID		4FSsp-QAAAAJ						
H-Index (As per SCOPUS Database)		4						
PROFESSIONAL MEMBERSHIPS		-						
Details of Short-Term Training Programs/Faculty Development Programs/Seminars/ Workshops (Attended)		• Received Certificate for participating in 3 days Capacity Development Program for ACADEMIC LEADERS & ADMINISTRATORS of Higher Educational Institutions and Universities organized by Institute for Academic Excellence (IAE) Hyderabad in collaboration with Commissionerate of Collegiate & Technical Education, Govt. of Telangana during 27 - 29 April 2023. • Received Certificate for participating in 2 days National Level Workshop on Curriculum Framework 2022 for Universities, Engineering Colleges and Degree Colleges from Mar-21st 2022 to Mar-22nd 2022. • Participated as a nominee member in All India Conference of Vice chancellors of universities offering Engineering and Technology programs during Apr-8th 2022 to Apr-9th 2022.						

	• Received Certificate for participating in 15 days faculty Training program-Abhigyat titled FPGA based VHDL design for advanced mobile algorithms & architectures from Dec-23rd 2017 to 10th Jan 2018. • Got Felicitated with certificate and reward for the excellent contribution in NBA Accreditation, UGC Autonomous inspection and NAAC Accreditation. • Contributed as a Reviewer for International Conference on Intelligent Communication, Control and Devices- ICICCD-2016 and ICICCD-2017. • Contributed as Session Chair in the track Intelligent Communication/ Intelligent Control/ Intelligent Devices for International Conference on Intelligent Communication, Control and Devices-ICICCD-2016 &2017. • Designed Surge Protection circuit in extension box and wireless Fan automation for Indo-Siemen Company, New-Delhi of worth Rs. 2 Lakhs • Award winners for the projects done under me by the students at RISE-Research Initiative for Students of Engineering for two consecutive years and still continuing in the coming year 2017 • Received certificate for participating a two week ISTE workshop titled" Control Systems (Dec 02-12, 2014)" under the National Mission on Education through ICT (MHRD, Govt. of. INDIA) conducted by IIT Kharagpur • Received certificate for participating a workshop titled" Short term course on Telecommunication Networks with State-of-the-Art Hands-On-Experiments (July 01-08, 2014)" organized by IIT Kharagpur • Got trained as an Assistant Professor for Teaching Methodology in National Institute of Technical Teachers Training & Research, Chennai. Also received certificate of training
Details of Short-Term Training Programs/Faculty Development Programs/Seminars/ Workshops (Organized)	• Conducted multiple Intensive Teaching Workshops to faculty covering Teaching, Learning and Discipline along with OBE, NEP concepts. • 7th July 2018, conducted a workshop titled "Digital Design with FPGA using Xilinx IP Cores under the IEEE & IETE student chapter, Telangana section. • Conducted a two-day workshop titled Internet of Things in collaboration with VINX, The Next Generation Solutions on 28th & 29th Sept. 2018. • Conducted a two-day workshop titled Speech Processing using MATLAB on 5th & 6th Oct 2018. With Dr. Anil Kumar, IIIT Hyderabad as the resource person • On 3rd February 2018 Organized a workshop titled "Digital Design with FPGA using Xilinx IP Cores under the IEEE student chapter Uttar Pradesh section. • Organized a workshop titled "Optical Communication and Networking" on September 10th and 11th 2014 under IEEE student chapter.