J.B. Institute of Engineering & Technology

Department of CSE

COURSE FILE

VLSI

Faculty

Srikanth

J.B. Institute of Engineering & Technology

Department of CSE

SYLLABUS

Subject Name: VLSI **Subject Code: VLSI**

Class : IV B.Tech. I Semester ECE **Faculty Name: Srikanth**

Sl.No	Unit #	Details of the unit
1	Introduction to IC Technology	MOS, PMOS, NMOS, CMOS & BiCMOS technologies- Oxidation, Lithography, Diffusion, Ion implantation, Metallization, Encapsulation, Probe testing, Integrated Resistors and Capacitors
2	BASIC ELECTRICAL PROPERTIES	Basic Electrical Properties of MOS and BiCMOS Circuits: Ids-Vds relationships, MOS transistor threshold Voltage, gm, gds, figure of merit. Pass transistor, NMOS Inverter, Various pull ups, CMOS Inverter analysis and design, Bi-CMOS Inverters.
3	VLSI CIRCUIT DESIGN PROCESSES	VLSI Design Flow, MOS Layers, Stick Diagrams, Design Rules and Layout, 2 um CMOS Design rules for wires, Contacts and Transistors Layout Diagrams for NMOS and CMOS Inverters and Gates, Scaling of MOS circuits, Limitations of Scaling.
4	GATE LEVEL DESIGN	Logic Gates and Other complex gates, Switch logic, Alternate gate circuits, Basic circuit concepts, Sheet Resistance RS and its concept to MOS, Area Capacitance Units, Calculations - Delays, Driving large Capacitive Loads, Wiring Capacitances, Fan-in and fan-out, Choice of layers
5	SUBSYSTEM DESIGN	Subsystem Design, Shifters, Adders, ALUs, Multipliers, Parity generators, Comparators, Zero/One Detectors, Counters, High Density Memory Elements.
6	SEMICONDUCTOR INTEGRATED CIRCUIT DESIGN	PLAs, FPGAs, CPLDs, Standard Cells, Programmable Array Logic, Design Approach.
7	VHDL SYNTHESIS	VHDL Synthesis, Circuit Design Flow, Circuit Synthesis, Simulation, Layout, Design capture tools, Design Verification Tools, Test Principles.
8		CMOS Testing, Need for testing, Test Principles,

	CMOS TESTING	Design Strategies for test, Chip level Test Techniques, System-level Test Techniques, Layout Design for improved Testability.

Text Book:

TB1. 1. Essentials of VLSI circuits and systems – Kamran Eshraghian, Eshraghian Dougles and A. Pucknell, PHI, 2005 Edition.
TB2. 2. Principles of CMOS VLSI Design - Weste and Eshraghian, Pearson Education, 1999

References:

RB1. 1. VLSI DESIGN by LAL KISHORE.

RB2. 2. CMOS VLSI DESIGN by Wayne wolf.

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SUBJECT PLAN

Subject Name: VLSI **Subject Code: VLSI**

Class : IV-B.Tech-Isem-IT **Faculty Name: Srikanth**

Unit #	Topics	Total No of Lessons
1	INTRODUCTION	08
2	BASIC ELECTRICAL PROPERTIES	08
3	VLSI CIRCUIT DESIGN PROCESSES	08
4	GATE LEVEL DESIGN	08
5	SUBSYSTEM DESIGN	08
6	SEMICONDUCTOR INTEGRATED CIRCUIT DESIGN	08
7	VHDL SYNTHESIS	08
8	CMOS TESTING	08
Total		**64**

- Each Period is of 50 Minutes. 5 periods each Week.

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LESSON PLAN

Subject Name: VLSI **Subject Code: VLSI**

Class : III B.Tech. II Semester CSE **Faculty Name: B.Kishore Kumar**

S.No	Topic as per JNTU syllabus	*Lesson s#	Suggested Books ** (Refer the list)	Question Bank			Hand outs
				OQ	DQ	AQ	
	Unit 1						
1	Introduction to IC Technology	2	TB1	OQ 1	DQ 1	A1	H1
2	MOS, PMOS, NMOS, CMOS & BiCMOS technologies	3	TB1			A1	
3	Oxidation, Lithography, Diffusion, Ion implantation, Metallization	3	RB1			A1	
	Unit 2						
4	Basic Electrical Properties of MOS and BiCMOS Circuits	2	TB1	OQ 1	DQ 1	A1	H2
5	Ids-Vds relationships, MOS transistor threshold Voltage, gm,	2	TB1			A1	

	gds, figure of merit						
6	Pass transistor, NMOS Inverter, Various pull ups	2	TB1			A1	
7	CMOS Inverter analysis and design, Bi-CMOS Inverters.	2	TB1			A1	
S.No	**Topic as per JNTU syllabus**	***Lesson s#**	**Suggested Books ** (Refer the list)**	**Question Bank** OQ DQ AQ			**Hand outs**
	Unit 3						
8	VLSI Design Flow, MOS Layers,	2	RB1	OQ 1	DQ 1	A1	H3
9	Stick Diagrams, Design Rules and Layout, 2	2	RB1			A1	
10	m CMOS Design rules for wires, Contacts and Transistors Layout Diagrams for NMOS and CMOS Inverters and Gates	2	TB1			A1	
11	Scaling of MOS circuits, Limitations of Scaling.	2	TB1			A1	
	Unit 4						
12	Logic Gates and Other complex gat	2	RB1	OQ 1	DQ 1	A1	H4
13	Switch logic, Alternate gate circuits	2	RB1			A1	
14	Time Delays, Driving large Capacit Loads, Wiring Capacitances	2	TB1			A1	
15	Fan in ,Fan out , Choice of layers	2	RB1			A1	
	Unit 5						
16	Subsystem Design	2	TB1	OQ 1	DQ 2	A2	H5
17	Subsystem Design, Shifters, Adders ALUs, Multipliers	2	TB1			A2	
18	Parity generators, Comparators,	2	TB1			A2	

	Zero/One Detectors						
19	Counters, High Density Memory Elements	2	TB1			A2	
S.No	**Topic as per JNTU syllabus**	***Lesson s#**	**Suggested Books ** (Refer the list)**	**Question Bank** OQ DQ AQ			**Hand outs**
	Unit 6			OQ 1	DQ 2		H6
20	Array Subsystems	2	RB1			A2	
21	SRAM,DRAM,ROM ,	2	RB1			A2	
22	Serial access memories	2	RB1			A2	
23	Content addressable memory	2	RB1			A2	
S.No	**Topic as per JNTU syllabus**	***Lesson s#**	**Suggested Books ** (Refer the list)**	**Question Bank** OQ DQ AQ			**Hand outs**
	Unit -7			OQ 1	DQ 2	A2	H7
24	Semiconductor Integrated Circuit Design	2	TB1			A2	
25	PLAs, FPGAs, CPLDs	2	TB1			A2	
26	Standard Cells, Programmable Arra Logic,	2	RB1			A2	
27	Design Approach	2	RB1			A2	
	Unit -8			OQ 1	DQ 2		H8
28	CMOS Testing, Need for testing, T Principles	2	TB1			A2	
29	Design Strategies for test, Chip leve Test Techniques	2	RB1			A2	
30	System-level Test Techniques,	2	RB1			A2	
31	Layout Design for improved Testability.	2	TB1			A2	
	Total Lessons	**64**					

Abbreviations and Notes

OQ: Objective Questions DQ: Descriptive Questions AQ: Assignment Questions

TB: Text Book RB: Reference Book SB: Suggested reference books (SB)

Text Book:

TB1: Essentials of VLSI circuits and systems – Kamran Eshraghian, Eshraghian Dougles and A. Pucknell, PHI, 2005 Edition

TB2: Principles of CMOS VLSI Design - Weste and Eshraghian, Pearson Education, 1999**.**

References:

RB1. 1. VLSI DESIGN by Lal Kishore.

RB2. 2. CMOS VLSI DESIGN by Wayne wolf.

Assignment No. 01

Class : III B.Tech. II Semester CSE VLSI

Objective:

1) What is Moore's law? Explain the evolution of IC technology?

2) Expalin the CMOS fabrication using n-Well and p-Well?

3) Explain the Bi-CMOS fabrication using n-Well process?

4) Explain drain characteristics of an n-channel enhancement MOSFET?

5) Define threshold voltage of an MOS device?

6) Explain the body effect of MOSFET?

7) What is the stick diagram? Draw various symbols for it.

8) Draw the stick diagram for nmos inverter?

9) Discuss the cmos design style?

10) Explain the clocked CMOS logic?

11) Compare the geometry aspects between 2-input NMOS NAND and CMOS NAND gates

Question No 1		**10 Marks**

1) Explain the steps involved in IC fabrication?

2) Explain the NMOS fabrication procedure?

3) Explain the Thermal oxidation technique and kinetics of thermal oxidation?

4) Describe the 3 sources of wiring capacitance?

5) Explain the effect of wiring capacitance on the performance of a VLSI circuit.

6) Explain the domino logic and n-p CMOS logic?

7) Design a layout diagram for pmosNAND?

8) What are the effects of scaling on Vt.

9) What are design rules? Why is metal-metal spacing larger than poly-poly spacing.

10) Derive an equation for Ids of an n-ch enhancement MOSFET operating in saturation region?

11) Explain channel length modulation of the MOSFET?

12) Explain the latch up problem in CMOS circuits?

13) Explain the transfer characteristics of a CMOS inverter?

14) Explain the steps involved in IC fabrication?

15) Explain the NMOS fabrication procedure?

16) Explain the Thermal oxidation technique and kinetics of thermal oxidation?

Question No 2	**10 Marks**

1) Explain the NMOS fabrication procedure?

2) Explain the Thermal oxidation technique and kinetics of thermal oxidation?

3) What is Moore's law? Explain the evolution of IC technology?

Assignment No. 02

Class : III B.Tech. II Semester CSE **Web Technologies**

Objectives

1) Draw the circuit diagram for 4-by-4 barrel shifter?

2) Explain the booth recorded multiplier?

3) Draw schematic for tiny XOR gate?

4) Explain the serial access memories?.

5) Content addressable memory?

6) Draw and explain the architecture for SRAM, DRAM, and ROM?

7) Write about channeled gate arrays.

8) Write about channeled gate arrays with neat sketch?

Question No 1		**10 Marks**

1) Explain the shifting operation for barrel shifter 4x4?

2) Explain the basic memory chip architecture?

3) Design a magnitude comparator based on the data path operation?

4) Draw the circuit diagram of one transistor with transistor capacitor dynamic RAM?

5) Explain the basic memory chip architecture**?**

6) Draw and explain the architecture of an FPGA?

7) What are the advantages and disadvantages of the reconfiguration?

8) Explain the gate level and function level of testing?

9) Draw the structure of parallel scan?

Question No 2	**10 Marks**

1) Design a magnitude comparator based on the data path operation?

2) Draw the circuit diagram of one transistor with transistor capacitor dynamic RAM?

VLSI : QUESTION BANK 1 (Objective)-OQ1

1) 1. The output of 3 iput OR gate when the inputs are 0,1and 0 is (**b**)

(a) 0

(b)1

(c) cannot be determined

(d) oscillating between 0, 1

2. Switch logic is based on? (**a**)

(a) pass transistor

(b) inverters

(c) gates

(d) nmos gates

3) Area capacitance is given by ? (**d)**

(a) C= eoA/D.

(b) C=e0/D

(c) C=A/D

(d) UML Profiles can be stereotyped for backward compatibility.

3). The n type pass transistor has length L=4λ,w= 2 λ Rs= ? (**b**)

most likely to be found in the main scenario of the use case ‘get drink’?

(a) – Rs

(b) 2Rs

(c) 3 Rs

(d) 4 Rs

4) The number of gates that can be connected at the input ? **(a)**
(a) Fan IN

(b) FAN OUT

(c) D C FAN OUT

(d) AC FANOUT

5) The yellow colour that is used in stickdiagram in NMOS design for? (**d**)

(a) N diffusion

(b) Polysilicon

(c) metal

(d) implant

6). The layers -------- at room temperature?

(a) lead oxide

(b) silicon oxide

(c) silicondioxide

(d) none

7). Inter layer capacitance is highly depended on.

(a) fringing field (**c**)

(b) layers.

(c) layout.

(d) wirelength.

8) For the 4X4 bit barrel shifter, the regularity factor is given by?

(a). 8.

(b) 4

(c) ‘2.

(d) ‘16.

9) The level of any particular design can be measured by (**c**)

(a) SNR

(b) Ratio of amplitude

(c) Regularity

(d) Quantity

10). The subsystem design is classified as

[a] first level

[b] top level

[c] bottom level

[d] leaf-cell level

11). A design that requires high density memory is

usually (**c**)

O (a. a single ship

b. on chip

c. partitioned into several chips

d. DRAMS

12)A CMOS PLA is realized by (**a**)
(a. pseudo nmos NOR gate

(b CMOS NOR gate

(c) pseudo nmos NAND gate.

(d) CMOS NAND gate.

13) The mapping of irregular combinational logic functions into regular structures is provided by the? [2 answers] (**d**)

[a] . FPGA.

[b]. CPCD.

[c] NAND/NOR structure

[d]. EX-OR/OR structure

14) V XP X Z PLA represents as? (**c**)

a. V-no.of input variables P-no.of output functions Z-no.of gates

b. V-no.of gates P-no.of OR gates Z- no.of AND gates

c. V-no.of input variables P-no.of product terms Z-no.of output functions

d. V-no.of gates P-no.of AND gates Z-no.of output functions

VLSI :QUESTION BANK 1 (Descriptive)-DQ1

) Explain the steps involved in IC fabrication?
2) Explain the NMOS fabrication procedure?
3) Explain the Thermal oxidation technique and kinetics of thermal oxidation?

4) Describe the 3 sources of wiring capacitance?

5) Explain the effect of wiring capacitance on the performance of a VLSI circuit.

6) Explain the domino logic and n-p CMOS logic?

7) Design a layout diagram for pmos NAND?

8) What are the effects of scaling on Vt.
9) What are design rules? Why is metal-metal spacing larger than poly-poly spacing.

10) Derive an equation for Ids of an n-ch enhancement MOSFET operating in saturation region?

11) Explain channel length modulation of the MOSFET?

12) Explain the latch up problem in CMOS circuits?

13) Explain the transfer characteristics of a CMOS inverter?

14) Explain the steps involved in IC fabrication?
15) Explain the NMOS fabrication procedure?
16) Explain the Thermal oxidation technique and kinetics of thermal oxidation?

VLSI: QUESTION BANK 3 (Descriptive)-DQ2

17)Explain the shifting operation for barrel shifter 4x4?

18) Explain the basic memory chip architecture?

19) Design a magnitude comparator based on the data path operation?

20) Draw the circuit diagram of one transistor with transistor capacitor dynamic RAM?

21) Explain the basic memory chip architecture**?**

22) Draw and explain the architecture of an FPGA?

23) What are the advantages and disadvantages of the reconfiguration?

24) Explain the gate level and function level of testing?
25) Draw the structure of parallel scan?