J.B. INSTITUTE OF ENGINEERING & TECHNOLOGY

(AUTONOMOUS)

ACADEMIC YEAR **2013-14**

http://www.jbiet.edu.in

	COURSE PLAN	2013-14
		Regulation: R11

FACULTY DETAILS:

Name of the Faculty:: P Kranthi Kumar
Designation: Asst .Professor
Department:: ECE

COURSE DETAILS

Name Of The Programme:: B.TECH Batch:: 2013-2014
Designation:: Asst.Professor
Year: IV Semester II
Department:: CSE
Title of The Subject VLSI Subject Code
No of Students 141

	COURSE PLAN	2013-14
		Regulation: R11

FACULTY DETAILS:

Name of the Faculty:: P KRANTHI KUMAR
Designation: Asst .Prof
Department:: ECE

1. TARGET

a) Percentage Pass: **85**

b) Percentage I class: **60**

2. COURSE PLAN

(Please write how you intend to cover the contents: i.e., coverage of Units by lectures, guest lectures, design exercises, solving numerical problems, demonstration of models, model preparation, or by assignments, etc.)

Indent to cover the contents of all units as per schedule by lectures, design exercises, solving problems, assignments, presentations, giving seminars etc... all are evaluated and done perfectly.

3. METHOD OF EVALUATION

3.1. ☐ Continuous Assessment Examinations (CAE 1, CAE 2) **10 marks**

3.2. ☐ **Assignments / Seminars 5 marks**

3.3. ☐ **Mini Projects**

3.4. ☐ **Quiz 5 marks**

3.5. ☐ Term End Examination **75 marks**

3.6. ☐ Others

4. List out any new topic(s) or any innovation you would like to introduce in teaching the subject in this Semester.

In the design of VLSIs, its goal is to implement higher integration and higher performance through the innovation of architecture, design tool and process technology. As the device minimum dimension becomes smaller below 100nm, diversified serious issues, including signal integrity and power dissipation, are being emerged. In order to overcome these barriers, the necessity of tight coupling, or effective joint activities which combine solutions of various layers between design and manufacturing fields

Signature of HOD
Date:

Signature of Faculty
Date:

	GUIDELINES TO STUDY THE SUBJECT	2013-14
		Regulation: R11

FACULTY DETAILS:

Name of the Faculty:: P KRANTHI KUMAR

Designation: ASST PROFESSOR

Department:: ECE

Guidelines for Preparing the Course: VLSI

Course Description:

The course will cover basic theory and techniques of digital VLSI design in CMOS technology. Topics include: CMOS devices and circuits, fabrication processes, static logic structures, chip layout, simulation and testing, low power techniques, design tools and methodologies, VLSI architecture. We use full-custom techniques to design basic cells and regular structures such as data-path and memory arrays. There is an emphasis on modern design issues in power, interconnect and clocking. We will also use several case-studies to explore recent real-world VLSI designs and papers from the recent research literature. Students will design and verify small test circuits using commercial CAD tools. Some final project designs may be fabricated and returned for testing.

Course Objectives:

1. This course should help student should be able to design and analyze digital circuits, incorporating into a VLSI chip.
2. They should be able to design for low power and design for performance, work in small groups and bring together design components into a full custom chip.
3. It is intended to provide students an understanding of various contemporary techniques for the design, Simulation.
4. Emphasis on full-custom design. – Circuit and system levels and and layout verification.
5. Specific techniques for designing high-speed, low-power, and easily-testable circuits
6. Students are also expected to understand various design methodologies such as custom, semi-custom, standard cell, arrayed logic, sea-of-gates.
7. A student is expected to be able to design and analyze digital circuits, understand transistor operations, circuit families.
8. To introduce students to basic concepts of digital VLSI chip design using the simpler VLSI technology.
9. To introduce the chip technology scaling process.
10. To understand cell library to be used by other chip designers.

Learning Outcomes:

A student who successfully fulfills the course requirements will have demonstrated:

1. Understand various VLSI processing techniques and fabrication principles.

2. Use mathematical methods and circuit analysis models in the analysis of CMOS digital electronics circuits.

3Convey knowledge of advanced concepts of circuit design for digital VLSI components in state of the art MOS technologies.

4. Create models of moderately sized CMOS circuits that realize specified digital functions.

5 .Design a circuit, build and optimize a CMOS layout.

6. Understand the concept of design flow in back end and front design including simulation, synthesis and design verification.

7. To test a combinational or sequential circuit.

8. To explain the challenges of current and future digital circuit design.

9. To complete a significant VLSI design project having a set of objective criteria and design constraints.

10.An ability to Specific techniques for designing high-speed, low-power, and easily-testable circuits

	COURSE OBJECTIVES	2013-14 REGULATION –R11

FACULTY DETAILS:

Name of the Faculty:: P KRANTHI KUMAR
Designation: Asst.Professor
Department:: ECE

On completion of this Subject / Course the student shall be able to:

S.No.	OBJECTIVES	OUTCOMES
1.	This course should help student should be able to design and analyze digital circuits, incorporating into a VLSI chip	Understand various VLSI processing techniques and fabrication principles.
2.	They should be able to design for low power and design for performance, work in small groups and bring together design components into a full custom chip.	Use mathematical methods and circuit analysis models in the analysis of CMOS digital electronics circuits
3.	Emphasis on full-custom design. – Circuit and system levels and and layout verification.	Convey knowledge of advanced concepts of circuit design for digital VLSI components in state of the art MOS technologies.
4.	Students are also expected to understand various design methodologies such as custom, semi-custom, standard cell, arrayed logic, sea-of-gates.	Create models of moderately sized CMOS circuits that realize specified digital functions.
5.	A student is expected to be able to design and analyze digital circuits, understand transistor operations, circuit families .	Design a circuit, build and optimize a CMOS layout.
6.	To introduce the chip technology scaling process	Understand the concept of design flow in back end and front design including simulation, synthesis and design verification.
7.	To understand cell library to be used by other chip designers.	To test a combinational or sequential circuit.
8.	It is intended to provide students an understanding of various contemporary techniques for the design, Simulation.	To explain the challenges of current and future digital circuit design.

.		To complete a significant VLSI design project having a set of objective criteria and design constraints.
9	To introduce data paths for microprocessors, including moderate-speed adders, subtracters, and multipliers.	
10.	To introduce the chip technology scaling process.	An ability to Specific techniques for designing high-speed, low-power, and easily-testable circuits

Signature of Faculty
Date:

Note: For each of the OBJECTIVE indicate the appropriate OUTCOMES to be achieved.
Kindly refer Page 16, to know the illustrative verbs that can be used to state the objectives.

	COURSE OUTCOMES	2013-14
		Regulation: R11

FACULTY DETAILS:

Name of the Faculty:: P KRANTHI KUMAR
Designation: Asst Prof
Department:: ECE

The expected outcomes of the Course / Subject are:

S.No	**General categories of outcomes**	**Specific outcomes of the course**
A	An ability to apply knowledge of mathematics, science, and engineering	Highly Related
B	An ability to design and conduct experiments, as well as to analyze and interpret data	Highly Related
C	An ability to design a system, component, or process to meet desired needs within realistic Constraints such as economic, environmental social, political, ethical, health and safety Manufacturability and sustainability	Supportive
D	An ability to function on multi-disciplinary teams	None
E	An ability to identify, formulate, and solve engineering problems	Highly Related
F	An understanding of professional and ethical responsibility	None
G	An ability to communicate effectively	Supportive
H	The broad education necessary to understand the impact of engineering solutions in a global, economic, environmental, and societal context	None
I	A recognition of the need for, and an ability to engage in life-long learning	Supportive
J	A knowledge of contemporary issues	None
K	An ability to use the techniques, skills, and modern engineering tools necessary for engineering practice.	Highly Related

Objectives – Outcome Relationship Matrix (Indicate the relationships by ☒ mark).

Outcomes / Objectives	A	B	C	D	E	F	G	H	I	J	K
1.	☒	☒	☒	☐	☒	☐	☒	☐	☒	☐	☒
2.	☒	☒	☒	☐	☒	☐	☒	☐	☐	☐	☒
3.	☒	☒	☒	☐	☒	☐	☒	☐	☐	☐	☒
4.	☒	☒	☐	☐	☒	☐	☐	☐	☐	☐	☒
5.	☒	☒	☒	☐	☒	☐	☒	☐	☒	☐	☒
6.	☒	☒	☒	☐	☒	☐	☒	☐	☐	☐	☒
7.	☒	☒	☐	☐	☒	☐	☐	☐	☒	☐	☒
8.	☒	☒	☐	☐	☒	☐	☐	☐	☐	☐	☒
9.	☒	☒	☐	☐	☒	☐	☐	☐	☐	☐	☒
10.	☒	☒	☒	☐	☒	☐	☒	☐	☐	☐	☒

	COURSE SCHEDULE	2013-14
		Regulation: R11

FACULTY DETAILS:

Name of the Faculty:: P KRANHI KUMAR
Designation: Asst Prof
Department:: ECE
The Schedule for the whole Course / Subject is:: VLSI

S. No.	DESCRIPTION	Duration (Date)		Total No. of Periods
		From	To	
1.	Introduction to IC Technology: MOS, PMOS, NMOS, CMOS & BiCMOS technologies-Oxidation, Lithography, Diffusion,Ionimplantation,Metallization, Encapsulation, Probe testing, Integrated Resistors and Capacitors	9/12/13	21/12/13	8
2.	Basic Electrical Properties of MOS and BiCMOSCircuits: Ids-Vds relationships, MOS transistor threshold Voltage, gm, gds, figure of merit. Pass transistor, NMOS Inverter, Various pull ups, CMOS Inverter analysis and design, Bi-CMOS Inverters.	23/12	2/1/14	8
3.	Vlsi Circuit Design Processes : VLSI Design Flow, MOS Layers, Stick Diagrams, Design Rules and Layout, 2 um CMOS Design rules for wires, Contacts and Transistors Layout Diagrams for NMOS and CMOS Inverters and Gates, Scaling of MOS circuits, Limitations of Scaling.	22/1/14	7/2/14	8
4.	Gate Level Design: Logic Gates and Other complex gates, Switch logic, Alternate gate circuits, Basic circuit concepts, Sheet Resistance RS and its concept to MOS, Area Capacitance Units, Calculations - Delays, Driving large Capacitive Loads, Wiring Capacitances, Fan-in and fan-out, Choice of layers	10/2/14	22/2/14	8
5.	Subsystem Design: Subsystem Design, Shifters, Adders, ALUs, Multipliers, Parity generators, Comparators, Zero/One Detectors, Counters, High Density Memory Elements.			

		24/2	5/3	8
6.	Semiconductor Integrated Circuit Design: PLAs, FPGAs, CPLDs, Standard Cells, Programmable Array Logic, Design Approach	7/3	15/3	8
7	Vhdl Synthesis: VHDL Synthesis, Circuit Design Flow, Circuit Synthesis, Simulation, Layout, Design capture tools, Design Verification Tools, Test Principles.	17/3	26/3	8
8	Cmos Testing: CMOS Testing, Need for testing, Test Principles, Design Strategies for test, Chip level Test Techniques, System-level Test Techniques, Layout Design for improved Testability.	28/3	7/3	8

Total No. of Instructional periods available for the course: Hours / Periods: 64

	SCHEDULE OF INSTRUCTIONS UNIT - I	2013-14 Regulation: R11

FACULTY DETAILS:

Name of the Faculty:: P KRANTHI KUMAR
Designation: Asst.Professor
Department:: ECE
The Schedule for the whole Course / Subject is::

Sl. No.	Date	No. of Periods	Topics / Sub - Topics	Objectives & Outcome Nos .	References (Text Book, Journal…) Page No___ to ___
1	9/12/14	1	Introduction VLSI	1,3,5,7,9& A,B, E,G,K	Essentials of VLSI circuits and systems KamranEshraghian, Eshraghian Dougles and A. Pucknell, PHI, 2005 Edition.
2	11/12/14	1	Introduction to IC Technology	1,3,5,7,9& A,B, E,G,K	DO
3	13/12/14	1	MOS, CMOS	1,3,5,7,9& A,B, E,G,K	DO
4	14/12/14	1	PMOS, NMOS technologies	1,3,5,7,9& A,B, E,G,K	DO
5	16/12/14	1	BiCMOS technologies	1,3,5,7,9& A,B, E,G,K	DO
6	18/12/14	1	Oxidation	1,3,5,7,9& A,B, E,G,K	DO
7	20/12/14	1	Lithography, Diffusion	1,3,5,7,9& A,B, E,G,K	DO
8	21/12/14	1	Ion implantation, Metallization	1,3,5,7,9& A,B, E,G,K	DO

Signature of Faculty
Date

Note: 1. ENSURE THAT ALL TOPICS SPECIFIED IN THE COURSE ARE MENTIONED.
2. ADDITIONAL TOPICS COVERED, IF ANY, MAY ALSO BE SPECIFIED **BOLDLY**.
3. MENTION THE CORRESPONDING COURSE OBJECTIVE AND OUT COME NUMBERS AGAINST EACH TOPIC.

	SCHEDULE OF INSTRUCTIONS UNIT - II	2013-14 Regulation: R11

FACULTY DETAILS:

Name of the Faculty:: P KRANTHI KUMAR
Designation: ASST.PROFESSOR
Department:: ECE
The Schedule for the whole Course / Subject is:: VLSI

Sl. No.	Date	No. of Periods	Topics / Sub - Topics	Objectives & Outcome Nos.	References (Text Book, Journal…) Page No___ to ___
1	23/12/14	1	Basic Electrical Properties of MOS	1,2,3,57,10,A,B,E,G,I,K	Essentials of VLSI circuits and systems KamranEshraghian, Eshraghian Dougles and A. Pucknell, PHI, 2005 Edition.
2	27/12/14	1	BiCMOS Circuits	1,2,3,57,10,A,B,E,G,I,K	DO
3	28/12/14	1	Ids-Vds relationships, MOS transistor threshold Voltage	1,2,3,57,10,A,B,E,G,I,K	DO
4	30/12/14	1	gm, gds, figure of merit	1,2,3,57,10,A,B,E,G,I,K	DO
5	1/1/14	1	Pass transistor, NMOS Inverter	1,2,3,57,10,A,B,E,G,I,K	DO
6	1/1/14	1	Various pull ups	1,2,3,57,10,A,B,E,G,I,K	DO
7	3/1/14	1	CMOS Inverter analysis and design	1,2,3,57,10,A,B,E,G,I,K	DO
8	20/1/14	1	Bi-CMOS Inverters	1,2,3,57,10,A,B,E,G,I,K	DO

Signature of Faculty
Date

Note: 1. ENSURE THAT ALL TOPICS SPECIFIED IN THE COURSE ARE MENTIONED.
2. ADDITIONAL TOPICS COVERED, IF ANY, MAY ALSO BE SPECIFIED **BOLDLY**.
3. MENTION THE CORRESPONDING COURSE OBJECTIVE AND OUT COME NUMBERS AGAINST EACH TOPIC.

	SCHEDULE OF INSTRUCTIONS UNIT - III	2013-14 Regulation: R11

FACULTY DETAILS:

Name of the Faculty:: P KRANTHI KUMAR
Designation: ASST.PROFESSOR
Department:: ECE
The Schedule for the whole Course / Subject is:: VLSI

SI. No.	Date	No. of Periods	Topics / Sub - Topics	Objectives & Outcome Nos.	References (Text Book, Journal…) Page No___ to ___
1	22/1/14	1	VLSI Design Flow	1,2,3,4&A,B,C,E,K,G	Essentials of VLSI circuits and systems KamranEshraghian, Eshraghian Dougles and A. Pucknell, PHI, 2005 Edition.
2	23/1/14	1	MOS Layers	1,2,3,4&A,B,C,E,K,G	DO
3	27/1/14	1	Stick Diagrams	1,2,3,4&A,B,C,E,K,G	DO
4	31/1/14	1	Design Rules and Layout	1,2,3,4&A,B,C,E,K,G	DO
5	1/2/14	1	2m CMOS Design rules for wires	1,2,3,4&A,B,C,E,K,G	DO
6	3/2/14	1	Contacts and Transistors Layout Diagrams for NMOS and CMOS Inverters and Gates	1,2,3,4&A,B,C,E,K,G	DO
7	5/2/14	1	Scaling of MOS circuits	1,2,3,4&A,B,C,E,K,G	DO
8	7/2/14	1	Limitations of Scaling.	1,2,3,4&A,B,C,E,K,G	DO

Signature of Faculty
Date

Note: 1. ENSURE THAT ALL TOPICS SPECIFIED IN THE COURSE ARE MENTIONED.
2. ADDITIONAL TOPICS COVERED, IF ANY, MAY ALSO BE SPECIFIED **BOLDLY**.
MENTION THE CORRESPONDING COURSE OBJECTIVE AND OUT COME NUMBERS AGAINST EACH TOPIC.

	SCHEDULE OF INSTRUCTIONS UNIT - IV	2013-14 Regulation: R11

FACULTY DETAILS:

Name of the Faculty:: P KRANTHI KUMAR
Designation: ASST PROFESSOR
Department:: ECE
The Schedule for the whole Course / Subject is:: VLSI

Sl. No.	Date	No. of Periods	Topics / Sub - Topics	Objectives & Outcome .	References (Text Book, Journal…) Page No___ to ___
1	10/2/14	1	Logic Gates	1,2,3,4,5,&,I, j, K,	Essentials of VLSI circuits and systems KamranEshraghian, Eshraghian Dougles and A. Pucknell, PHI, 2005 Edition.
2	11/2/14	1	Other complex gates	1,2,3,4,5,& I, j, K,	DO
3	12/2/14	1	Switch logic	1,2,3,4,5,&,I, j, K	DO
4	14/2/14	1	Alternate gate circuits	1,2,3,4,5,&,I, j, K	DO
5	15/2/14	1	Time Delays, Driving large Capacitive Loads,	1,2,3,4,5,&, I, j, K	DO
6	19/2/14	1	Wiring Capacitances	1,2,3,4,5,& I, j, K	DO
7	21/2/14	1	Fan in ,Fan out ,	1,2,3,4,5,&,I, j, K,	DO
8	22/2/14	1	Choice of layers	1,2,3,4,5,& I, j, K,	DO

Signature of Faculty
Date

Note: 1. ENSURE THAT ALL TOPICS SPECIFIED IN THE COURSE ARE MENTIONED.
2. ADDITIONAL TOPICS COVERED, IF ANY, MAY ALSO BE SPECIFIED **BOLDLY**.
MENTION THE CORRESPONDING COURSE OBJECTIVE AND OUT COME NUMBERS AGAINST EACH TOPIC.

	SCHEDULE OF INSTRUCTIONS UNIT - V	2013-14 Regulation: R11

FACULTY DETAILS:

Name of the Faculty:: P KRANTHI KUMAR
Designation: Asst.Professor
Department:: ECE
The Schedule for the whole Course / Subject is:: VLSI

Sl. No.	Date	No. of Periods	Topics / Sub - Topics	Objectives & Outcome Nos.	References (Text Book, Journal…) Page No___ to ___
1	24/2/14	1	Subsystem Design	1,3,5,7&A,B,C,E,K,I	Essentials of VLSI circuits and systems Kamran Eshraghian, Eshraghian Dougles and A. Pucknell, PHI, 2005 Edition.
2	26/2/14	1	Contin...Subsystem Design	1,3,5,7&A,B,C,E,K,I	DO
3	26/2/14	1	Subsystem Design, Shifters,	1,3,5,7&A,B,C,E,K,I	DO
4	28/2/14	1	Adders, ALUs, Multipliers	1,3,5,7&A,B,C,E,K,I	DO
5	1/3/14	1	Parity generators, Comparators,	1,3,5,7&A,B,C,E,K,I	DO
6	3/3/14	1	Zero/One Detectors	1,3,5,7&A,B,C,E,K,I	DO
7	5/3/14	1	Counters	1,3,5,7&A,B,C,E,K,I	DO
8	5/3/14	1	High Density Memory Elements	1,3,5,7&A,B,C,E,K,I	DO

Signature of Faculty
Date

Note: 1. ENSURE THAT ALL TOPICS SPECIFIED IN THE COURSE ARE MENTIONED.
2. ADDITIONAL TOPICS COVERED, IF ANY, MAY ALSO BE SPECIFIED **BOLDLY**.
MENTION THE CORRESPONDING COURSE OBJECTIVE AND OUT COME NUMBERS AGAINST EACH TOPIC.

	SCHEDULE OF INSTRUCTIONS UNIT - VI	2013-14 Regulation: R11

FACULTY DETAILS:

Name of the Faculty:: P KRANTHI KUMAR
Designation: Asst .Professor
Department:: ECE
The Schedule for the whole Course / Subject is:: VLSI

SI. No.	Date	No. of Periods	Topics / Sub - Topics	Objectives & Outcome Nos	References (Text Book, Journal…) Page No___ to ___
1	7/3/14	1	Array Subsystems	2,3,4,5,8&A,B,C,E,G,K	Essentials of VLSI circuits and systems KamranEshraghian, Eshraghian Dougles and A. Pucknell, PHI, 2005 Edition.
2	8/3/14	1	Contin...Array Subsystems	2,3,4,5,8&A,B,C,E,G,K	DO
3	10/3/14	1	SRAM,DRAM	2,3,4,5,8&A,B,C,E,G,K	DO
4	12/3/14	1	ROM	2,3,4,5,8&A,B,C,E,G,K	DO
5	12/3/14	1	Serial access memories	2,3,4,5,8&A,B,C,E,G,K	DO
6	14/3/14	1	Contin...Serial access memo	2,3,4,5,8&A,B,C,E,G,K	DO
7	15/3/14	1	Content addressable memory	2,3,4,5,8&A,B,C,E,G,K	DO
8	15/3/14	1	Contin...Content addressable memory	2,3,4,5,8&A,B,C,E,G,K	DO

Signature of Faculty
Date

Note: 1. ENSURE THAT ALL TOPICS SPECIFIED IN THE COURSE ARE MENTIONED.
2. ADDITIONAL TOPICS COVERED, IF ANY, MAY ALSO BE SPECIFIED **BOLDLY**.
3. MENTION THE CORRESPONDING COURSE OBJECTIVE AND OUT COME NUMBERS AGAINST EACH TOPIC

	SCHEDULE OF INSTRUCTIONS UNIT - VII	2013-14 Regulation: R11

FACULTY DETAILS:

Name of the Faculty:: P KRANTHI KUMAR
Designation: ASST PROFESSOR
Department:: ECE
The Schedule for the whole Course / Subject is:: VLSI

SI. No.	Date	No. of Periods	Topics / Sub - Topics	Objectives & Outcome Nos.	References (Text Book, Journal…) Page No___ to ___
1	17/3/14	1	Semiconductor Integrated Circuit Design	2,3,4,5,8&A,B,C,E,G,K	Essentials of VLSI circuits and systems KamranEshraghian, Eshraghian Dougles and A. Pucknell, PHI, 2005 Edition.
2	19/3/14	1	Semiconductor Integrated Circuit Design Contin....	2,3,4,5,8&A,B,C,E,G,K	DO
3	19/3/14	1	PLAs, FPGAs	2,3,4,5,8&A,B,C,E,G,K	DO
4	21/3/14	1	CPLDs	2,3,4,5,8&A,B,C,E,G,K	DO
5	22/3/14	1	Standard Cells,	2,3,4,5,8&A,B,C,E,G,K	DO
6	24/3/14	1	Programmable Array Logic,	2,3,4,5,8&A,B,C,E,G,K	DO
7	26/3/14	1	Design Approach	2,3,4,5,8&A,B,C,E,G,K	DO
8	26/3/14	1	Design Approach contin.....	2,3,4,5,8&A,B,C,E,G,K	DO

Signature of Faculty
Date

Note:1. ENSURE THAT ALL TOPICS SPECIFIED IN THE COURSE ARE MENTIONED.
2. ADDITIONAL TOPICS COVERED, IF ANY, MAY ALSO BE SPECIFIED **BOLDLY**.
3. MENTION THE CORRESPONDING COURSE OBJECTIVE AND OUT COME NUMBERS AGAINST EACH TOPIC

	SCHEDULE OF INSTRUCTIONS UNIT - VIII	2013-14 Regulation: R11

FACULTY DETAILS:

Name of the Faculty:: P KRANTHI KUMAR
Designation: Asst Professor
Department:: ECE
The Schedule for the whole Course / Subject is:: VLSI

Sl. No.	Date	No. of Periods	Topics / Sub - Topics	Objectives & Outcome Nos.	References (Text Book, Journal…) Page No___ to ___
1	28/3/14	1	CMOS Testing	1,2,3,4,5,&A,B,E,G, K,	Essentials of VLSI circuits andsystemsKamranEshraghian, Eshraghian Dougles and A. Pucknell, PHI, 2005 Edition.
2	29/3/14	1	Need for testing, Test Principles	1,2,3,4,5,&A,B,E,G, K,	DO
3	31/3/14	1	Design Strategies for test	1,2,3,4,5,&A,B,E,G, K,	DO
4	2/4/14	1	Chip level Test Techniques	1,2,3,4,5,&A,B,E,G, K,	DO
5	2/4/14	1	System-level Test Techniques,	1,2,3,4,5,&A,B,E,G, K,	DO
6	4/4/14	1	System-level Test Techniques contin	1,2,3,4,5,&A,B,E,G, K,	DO
7	5/4/14	1	Layout Design for improved Testability.	1,2,3,4,5,&A,B,E,G, K,	DO
8	7/4/14	1	Layout Design for improved Testability. contin.....	1,2,3,4,5,&A,B,E,G, K,	DO

Signature of Faculty
Date

Note: 1. ENSURE THAT ALL TOPICS SPECIFIED IN THE COURSE ARE MENTIONED.
2. ADDITIONAL TOPICS COVERED, IF ANY, MAY ALSO BE SPECIFIED **BOLDLY**.
MENTION THE CORRESPONDING COURSE OBJECTIVE AND OUT COME NUMBERS AGAINST EACH TOPIC.

	COURSE COMPLETION STATUS	2013-14
		Regulation: R11

FACULTY DETAILS:

Name of the Faculty:: P KRANTHI KUMAR
Subject: VLSI Subject Code:
Department:: ECE

Actual Date of Completion & Remarks, if any

Units	Remarks	Nos. of Objectives Achieved
Unit 1	**Successfully completed this unit along with unsolved and solved numerical problems**	**5**
Unit 2	**Successfully completed this unit along with unsolved and solved numerical problems**	**6**
Unit 3	**Successfully completed this unit along with unsolved and solved numerical problems**	**4**
Unit 4	**Successfully completed this unit along with unsolved and solved numerical problems**	**5**
Unit 5	**Successfully completed this unit along with unsolved and solved numerical problem**	**4**
Unit 6	**Successfully completed this unit along with unsolved and solved numerical problems**	**5**
Unit 7	**Successfully completed this unit along with unsolved and solved numerical problems**	**5**
Unit 8	**Successfully completed this unit along with unsolved and solved numerical problems**	**5**

Signature of Dean of School
Date:

Signature of Faculty
Date:

NOTE: AFTER THE COMPLETION OF EACH UNIT MENTION THE NUMBER OF OBJECTIVES ACHIEVED.

	TUTORIAL SHEETS - I	2013-14
		Regulation: R11

FACULTY DETAILS:

Name of the Faculty:: P KRANTHI KUMAR
Designation: ASST PROFESSOR
Department:: ECE
The Schedule for the whole Course / Subject is::

Date: **Date: 31/07/13**

This Tutorial corresponds to Unit Nos. **01, 02,03,4 & 5**

Time: **Time: 10:30AM**

Q1. What is Moore's law? Explain the evolution of IC technology?

Q2. Derive an equation for Ids of an n-ch enhancement MOSFET operating in saturation region?

Q3. Draw schematic for tiny XOR gate?

Q4. Explain the booth recorded multiplier?

Q5. Explain the serial access memories?.

Please write the Questions / Problems / Exercises which you would like to give to the students and also mention the objectives to which these questions / Problems are related.

Signature of Dean of School
Date:

Signature of Faculty
Date:

	TUTORIAL SHEETS - II	2013-14
		Regulation: R11

FACULTY DETAILS:

Name of the Faculty:: P KRANTHI KUMAR
Designation: ASST PROFESSOR
Department:: ECE
The Schedule for the whole Course / Subject is::

Date:16/08/13

This Tutorial corresponds to Unit Nos. **01,02,03,04**

Time:12:30PM

Q1. Explain the steps involved in IC fabrication?

Q2. Determine the pull up to pull down ratio of an n-mos inverter driven by another n-mos inverter?

Q3. Draw the stick diagram for two i/p CMOS NOR Gate.

Q4. Explain the 'switch logic'in detail for building logic circuits

Q5. Design a magnitude comparator based on the data path operation?

Please write the Questions / Problems / Exercises which you would like to give to the students and also mention the objectives to which these questions / Problems are related.

Signature of Dean of School
Date:

Signature of Faculty
Date:

	TUTORIAL SHEETS - III	2013-14
		Regulation: R11

FACULTY DETAILS:

Name of the Faculty:: P KRANTHI KUMAR
Designation: ASST PROFESSOR
Department:: ECE

Date:8/10/2013

This Tutorial corresponds to Unit Nos. **06,7,08**

Time:9:30AM

1. a)Explain about
   i) Carry Ripple Adder
   ii) Carry Lookahead Adder

   b)Explain Booth recording procedure with an example in array multiplier?

2. Discuss about shift Registers with neat diagrams?

3. Discuss about principle and operation of the following:

   i) FPGA

   II) CPLD

4.a) Explain about different fault models in VLSI testing with an example?

   b) Explain the Scan path design technique used to test sequential circuit indetail.

Please write the Questions / Problems / Exercises which you would like to give to the students and also mention the objectives to which these questions / Problems are related.

Signature of Dean of School
Date:

Signature of Faculty
Date:

	ILLUSTRATIVE VERBS FOR STATING INSTRUCTIONAL OBJECTIVES	2013-14
		Regulation: R11

These verbs can also be used while framing questions for Continuous Assessment Examinations as well as for End – Semester (final) Examinations.

ILLUSTRATIVE VERBS FOR STATING **GENERAL OBJECTIVES**

Know Comprehend	Understand Apply	Analyze Design	Generate Evaluate

ILLUSTRATIVE VERBS FOR STATING **SPECIFIC OBJECTIVES:**

A. Cognitive Domain

1	2	3	4	5	6
Knowledge	**Comprehension Understanding**	**Application** of knowledge & comprehension	**Analysis** of whole w.r.t. its constituents	**Synthesis** combination of ideas/constituents	**Evaluation** judgement
Define	Convert	Change	Breakdown	Categorize	Appraise
Identify	Defend	Compute	Differentiate	Combine	Compare
Label	Describe (a	Demonstrate	Discriminate	Compile	Conclude
List	procedure)	Deduce	Distinguish	Compose	Contrast
Match	Distinguish	Manipulate	Separate	Create	Criticize
Reproduce	Estimate	Modify	Subdivide	Devise	Justify
Select	Explain why/how	Predict		Design	Interpret
State	Extend	Prepare		Generate	Support
	Generalize	Relate		Organize	
	Give examples	Show		Plan	
	Illustrate	Solve		Rearrange	
	Infer			Reconstruct	
	Summarize			Reorganize	
				Revise	

B. Affective Domain		**C. Psychomotor Domain (skill development)**				
Adhere	Resolve	Bend	Dissect	Insert	Perform	Straighten
Assist	Select	Calibrate	Draw	Keep	Prepare	Strengthen
Attend	Serve	Compress	Extend	Elongate	Remove	Time
Change	Share	Conduct	Feed	Limit	Replace	Transfer
Develop		Connect	File	Manipulate	Report	Type
Help		Convert	Grow	Move preciselyReset		Weigh
Influence		Decrease	Handle	Operate	Run	
Initiate		Demonstrate	Increase	Paint	Set	

	LESSON PLAN Unit-1	2013-14
		Regulation: R11

Name of the Faculty: P KRANTHI KUAMR

Subject VLSI Subject Code **6757035**

Unit 1

INSTRUCTIONAL OBJECTIVES:

Session No	Topics to be covered	Time	Ref	Teaching Method
1	**Introduction VLSI**	**50 MIN**	**Essentials of VLSI circuits and systems KamranEshraghian, Eshraghian Dougles and A. Pucknell, PHI, 2005 Edition**	**Black Board**
2	**Introduction to IC Technology**	**50 MIN**	**do**	**Black Board**
3	**MOS, CMOS**	**50 MIN**	**do**	**Black Board**
4	**PMOS, NMOS technologies**	**50 MIN**	**do**	**Black Board**
5	**BiCMOS technologies**	**50 MIN**	**do**	**Black Board**
6	**Oxidation**	**50 MIN**	**do**	**Black Board**
7	**Lithography, Diffusion**	**50 MIN**	**do**	**Black Board**
8	**Ion implantation, Metallization**	**50 MIN**	**do**	**Black Board**

On completion of this lesson the student shall be able to(Outcomes)

1. An ability to Specific techniques for designing high-speed, low-power, and easily-testable circuits
2. An ability to estimate and compute the power consumption of a VLSI chip.
3. An ability to analyze VLSI circuit timing using Logical Effort analysis.
4. An ability to extract the analog parasitic elements from the layout and analyze the circuit timing using a logic simulator and an analog simulator.

	ASSIGNMENT **Unit-I**	2013-14
		Regulation: R11

Assignment / Questions

1) What is Moore's law? Explain the evolution of IC technology?

2) Expalin the CMOS fabrication using n-Well and p-Well?

3) Explain the Bi-CMOS fabrication using n-Well process?

4) Explain drain characteristics of an n-channel enhancement MOSFET?

5) Define threshold voltage of an MOS device?

Signature of Faculty

Note: Mention for each question the relevant objectives and outcomes.

1. This course should help student should be able to design and analyze digital circuits, incorporating into a VLSI chip.
2 They should be able to design for low power and design for performance, work in small groups and bring together design components into a full custom chip.
3. It is intended to provide students an understanding of various contemporary techniques for the Design, Simulation.
4.Emphasis on full-custom design. – Circuit and system levels and and layout verification.
5 Specific techniques for designing high-speed, low-power, and easily-testable circuits

	LESSON PLAN **Unit-II**	2013-14 Regulation: R11

Name of the Faculty: P KRANTHI KUMAR

Subject : VLSI Subject Code **6757035**

Unit : 2

INSTRUCTIONAL OBJECTIVES:

Session No	Topics to be covered	Time	Ref	Teaching Method
1	**Basic Electrical Properties of MOS**	50 MIN	**Essentials of VLSI circuits and systems KamranEshraghian, Eshraghian Dougles and A. Pucknell, PHI, 2005 Edition.**	**Black Board**
2	**BiCMOS Circuits**	50 MIN	**DO**	**Black Board**
3	**Ids-Vds relationships, MOS transistor threshold Voltage**	50 MIN	**DO**	**Black Board**
4	**gm, gds, figure of merit**	50 MIN	**DO**	**Black Board**
5	**Pass transistor, NMOS Inverter**	50 MIN	**DO**	**Black Board**
6	**Various pull ups**	50 MIN	**DO**	**Black Board**
7	**CMOS Inverter analysis and design**	50 MIN	**DO**	**Black Board**
8	**Bi-CMOS Inverters**	50 MIN	**DO**	**Black Board**
9	**Basic Electrical Properties of MOS**	50 MIN	**DO**	**Black Board**

On completion of this lesson the student shall be able to

1. An ability to extract the analog parasitic elements from the layout and analyze the circuit timing using a logic simulator and an analog simulator.

2. An ability to analyze vlsi circuit timing using logical effort analysis.

3. An ability to analyze electrical properties of mos.
4. An ability to design the circuits using cmos invertor.

	ASSIGNMENT **Unit-II**	2013-14 Regulation: R11

Assignment / Questions

1. Derive an equation for Ids of an n-ch enhancement MOSFET operating in saturation region?
2. Define the relation between Ids and Vds of MOSFET in non-saturation region?
3. Determine the pull up to pull down ratio of an n-mos inverter driven by another n-mos inverter?
4. Explain the CMOS Inverter analysis and design in details.
5. Explain the Bi-CMOS Inverters in brief.

Signature of Faculty

Note: Mention for each question the relevant objectives and outcomes.

1. An ability to extract the analog parasitic elements from the layout and analyze the circuit timing using a logic simulator and an analog simulator.

2.Specific techniques for designing high-speed, low-power, and easily-testable circuits.

	LESSON PLAN Unit-III	2013-14 Regulation: R11

Name of the Faculty: P KRANTHI KUMAR

Subject VLSI Subject Code **6757035**

Unit 3

INSTRUCTIONAL OBJECTIVES:

Session No	Topics to be covered	Time	Ref	Teaching Method
1	VLSI Design Flow	50 MIN	Essentials of VLSI circuits and systems KamranEshraghian, Eshraghian Dougles and A. Pucknell, PHI, 2005 Edition.	Black Board
2	MOS Layers	50 MIN	DO	Black Board
3	Stick Diagrams	50 MIN	DO	Black Board
4	Design Rules and Layout	50 MIN	DO	Black Board
5	2m CMOS Design rules for wires	50 MIN	DO	Black Board
6	Contacts and Transistors Layout Diagrams for NMOS and CMOS Inverters and Gates	50 MIN	DO	Black Board
7	Scaling of MOS circuits	50 MIN	DO	Black Board
8	Limitations of Scaling.	50 MIN	DO	Black Board

On completion of this lesson the student shall be able to(Outcomes)

1. An ability to estimate and compute the power consumption of a VLSI chip.
2. An ability to assemble an entire chip and add the appropriate pads to a layout
3. An ability to explain the chip technology scaling process.
4. An ability to analyze VLSI circuit timing using Logical Effort analysis.

	ASSIGNMENT **Unit-III**	2013-14 Regulation: R11

Assignment / Questions

1. a) Give the color encoding for various layers for MOS transistors.
   b) Draw the stick diagram for two i/p CMOS NOR Gate.
2. Draw the layout diagram for CMOS NAND gate.
3. Explain the stick diagram for NAND,NOR using nmos,pmos style.
4. Explain the Scaling of MOS circuits in detail.
5. Explain the 2m CMOS Design rules for wires in brief.

Signature of Faculty

Note: Mention for each question the relevant objectives and outcomes.

1. An ability to analyze vlsi circuit timing using logical effort analysis.
2. An ability to assemble an entire chip and add the appropriate pads to a layout

	LESSON PLAN Unit-IV	2013-14
		Regulation: R11

Name of the Faculty: P KRANTHI KUMAR

Subject VLSI Subject Code **6757035**

Unit 4

INSTRUCTIONAL OBJECTIVES:

Session No	Topics to be covered	Time	Ref	Teaching Method
1	**Logic Gates**	**50 MIN**	**Essentials of VLSI circuits and systems KamranEshraghian, Eshraghian Dougles and A. Pucknell, PHI, 2005 Edition.**	**Blackboard**
2	**Other complex gates**	**50 MIN**	**DO**	**Blackboard**
3	**Switch logic**	**50 MIN**	**DO**	**Blackboard**
4	**Alternate gate circuits**	**50 MIN**	**DO**	**Blackboard**
5	**Time Delays, Driving large Capacitive Loads,**	**50 MIN**	**DO**	**Blackboard**
6	**Wiring Capacitances**	**50 MIN**	**DO**	**Blackboard**
7	**Fan in ,Fan out ,**	**50 MIN**	**DO**	**Blackboard**
8	**Choice of layers**	**50 MIN**	**DO**	**Blackboard**

On completion of this lesson the student shall be able to (Outcomes)

1. An ability to Specific techniques for designing high-speed, low-power, and easily-testable circuits
2. An ability to analyze VLSI gate logic design with effortlessly.
3. An ability to assemble an entire chip and add the appropriate pads to a layout
4. An ability to analyse the choice of layers according to design.

	ASSIGNMENT **Unit-IV**	2013-14
		Regulation: R11

Assignment / Questions

1.Explain the 'Pass transistors and Transmission Gates 'in detail for building logic circuits.

2.Explain the 'switch logic'in detail for building logic circuits.

3. Explain the large Capacitive Loads in breif

4. Explain the types of the Wiring Capacitances.

5. Explain the Time Delays introduce in pass transistor in details?

Signature of Faculty

Note: Mention for each question the relevant objectives and outcomes.

1. An ability to analyze VLSI gate logic design with effortlessly .

2. It is intended to provide students an understanding of various contemporary techniques for the Design, Simulation.

	LESSON PLAN Unit-V	2013-14
		Regulation: R11

Name of the Faculty: P KRANTHI KUMAR

Subject VLSI Subject Code **6757035**

Unit 5

INSTRUCTIONAL OBJECTIVES:

Session No	Topics to be covered	Time	Ref	Teaching Method
1	**Subsystem Design**	50 MIN	**Essentials of VLSI circuits and systems KamranEshraghian, Eshraghian Dougles and A. Pucknell, PHI, 2005 Edition.**	**Black Board**
2	**Contin...Subsystem Design**	50 MIN	DO	**Black Board**
3	**Subsystem Design, Shifters**	50 MIN	DO	**Black Board**
4	**Adders, ALUs, Multipliers**	50 MIN	DO	**Black Board**
5	**Parity generators, Comparators**	50 MIN	DO	**Black Board**
6	**Zero/One Detectors**	50 MIN	DO	**Black Board**
7	**Counters**	50 MIN	DO	**Black Board**
8	**High Density Memory Elements**	50 MIN	DO	**Black Board**

On completion of this lesson the student shall be able to (Outcomes)

1. An ability to insert elementary logic testing hardware into the VLSI chip.
2. An ability to estimate and compute the power consumption of a VLSI chip
3. An ability to apply the concepts based on subsystem design
4. An ability to Specific techniques for designing high-speed, low-power, and easily-testable circuits

	ASSIGNMENT **Unit-V**	2013-14 Regulation: R11

Assignment / Questions

1. Explain about
   a) Carry Ripple Adder
   b) Carry Look ahead Adder
   c) Explain Booth recording procedure with an example in array multiplier?
2. Discuss about shift Registers with neat diagrams?
3. Explain the Wall trace Multiplier?
4. Explain the types of the Counters in detail.
5. Explain the magnitude Comparator with an example.

Signature of Faculty

Note: Mention for each question the relevant objectives and outcomes.

1.It is intended to provide students an understanding of various contemporary techniques for the Design, Simulation.

2.An ability to apply the concepts based on subsystem design

	LESSON PLAN **Unit-VI**	2013-14 Regulation: R11

Name of the Faculty:

Subject Subject Code **6757035**

Unit

INSTRUCTIONAL OBJECTIVES:

Session No	Topics to be covered	Time	Ref	Teaching Method
1	**Array Subsystems**	**50 MIN**	**Essentials of VLSI circuits and systems KamranEshraghian, Eshraghian Dougles and A. Pucknell, PHI, 2005 Edition.**	**Black Board**
2	**Contin...Array Subsystems**	**50 MIN**	**DO**	**Black Board**
3	**SRAM,DRAM**	**50 MIN**	**DO**	**Black Board**
4	**ROM**	**50 MIN**	**DO**	**Black Board**
5	**Serial access memories**	**50 MIN**	**DO**	**Black Board**
6	**Contin...Serial access memories**	**50 MIN**	**DO**	**Black Board**
7	**Content addressable memory**	**50 MIN**	**DO**	**Black Board**
8	**Contin...Content addressable memory**	**50 MIN**	**DO**	**Black Board**

On completion of this lesson the student shall be able to (Outcomes)

1. An ability to design elementary data paths for microprocessors, including memory array subsystems,moderate-speed adders, subtracters, and multipliers.

2. An ability to Specific techniques for designing high-speed, low-power.

3. An ability to analyze VLSI circuit timing using Logical Effort analysis.

4. An ability to assemble an entire chip and add the appropriate pads to a layout

	ASSIGNMENT **Unit-VII**	2013-14 Regulation: R11

Assignment / Questions

1 Explain the Serial access memories with examples.

2 Explain the Content addressable memory with examples.

3 Explain the Array Subsystems in brief.

4 Explain the types of DRAM in detai?

Signature of Faculty

Note: Mention for each question the relevant objectives and outcomes.

1.It is intended to provide students an understanding of various contemporary techniques for the Design, Simulation

2. An ability to analyze VLSI circuit timing using Logical Effort analysis.

	LESSON PLAN Unit-VII	2013-14
		Regulation: R11

Name of the Faculty: P KRANTHI KUMAR

Subject VLSI Subject Code **6757035**

Unit 7

INSTRUCTIONAL OBJECTIVES:

Session No	Topics to be covered	Time	Ref	Teaching Method
1	**Semiconductor Integrated Circuit Design**	50 MIN	**Essentials of VLSI circuits and systems KamranEshraghian, Eshraghian Dougles and A. Pucknell, PHI, 2005 Edition.**	Black Board
2	**Semiconductor Integrated Circuit Design Contin....**	50 MIN	DO	Black Board
3	**PLAs, FPGAs**	50 MIN	DO	Black Board
4	**CPLDs**	50 MIN	DO	Black Board
5	**Standard Cells**	50 MIN	DO	Black Board
6	**Programmable Array Logic**	50 MIN	DO	Black Board
7	**Design Approach**	50 MIN	DO	Black Board
8	**Design Approach contin.....**	50 MIN	DO	Black Board

On completion of this lesson the student shall be able to

1. An ability to explain the chip design.

2. An ability to insert elementary testing hardware FPGA into the VLSI chip.

3. An ability to design Standard cells according to IC design.

4. An ability to Specific techniques for designing high-speed, low-power, and easily-testable circuits.

	ASSIGNMENT **Unit-VII**	2013-14 Regulation: R11

Assignment / Questions

1. Discuss about principle and operation of the following:
   i) FPGA
   ii) CPLD

2. (a) What is the goal of VHDL synthesis step in design flow?
   (b) Explain how register transfer level description provides optimized synthesis netlist.
3. What is need for RTL simulation? Clearly explain RTL simulation flow in the ASIC design flow and also mention few leading simulation tools.

Signature of Faculty

Note: Mention for each question the relevant objectives and outcomes.

1. It is intended to provide students an understanding of various contemporary techniques for the Design, Simulation

2. An ability to design Standard cells according to IC design.

	LESSON PLAN **Unit-VIII**	2013-14 Regulation: R11

Name of the Faculty: G Sreenivasulu

Subject Web Technologies Subject Code **6757035**

Unit VIII

INSTRUCTIONAL OBJECTIVES:

Session No	Topics to be covered	Time	Ref	Teaching Method
1	**CMOS Testing**	50 MIN	**Essentials of VLSI circuits and systems KamranEshraghian, Eshraghian Dougles and A. Pucknell, PHI, 2005 Edition.**	**Black Board**
2	**Need for testing, Test Principles**	50 MIN	DO	**Black Board**
3	**Design Strategies for test**	50 MIN	DO	**Black Board**
4	**Chip level Test Techniques**	50 MIN	DO	**Black Board**
5	**System-level Test Techniques,**	50 MIN	DO	**Black Board**
6	**System-level Test Techniques continue..**	50 MIN	DO	**Black Board**
7	**Layout Design for improved Testability.**	50 MIN	DO	**Black Board**
8	**Layout Design for improved Testability. contin.....**	50 MIN	DO	**Black Board**

On completion of this lesson the student shall be able to

1. An ability to insert elementary testing hardware into the VLSI chip
2. An ability to estimate and compute the power consumption of a VLSI chip
3. An ability to apply various strategies for the CMOS testing.
4. An ability to design elementary and can improve testability of CMOS design.

	ASSIGNMENT **Unit-VIII**	2013-14 Regulation: R11

Assignment / Questions

1. Explain about different fault models in VLSI testing with an example?
2. Explain the Scan path design technique used to test sequential circuit indetail.
3. Explain the System-level Test Techniques in detail.
4. Explain the Chip level Test Techniques in detail.
5. Explain the Need for testing how it is used in VLSI techniques.

Signature of Faculty

Note: Mention for each question the relevant objectives and outcomes.

1. An ability to estimate and compute the power consumption of a VLSI chip
2. It is intended to provide students an understanding of various contemporary techniques for the Design, Simulation