JBIET Academic Regulations - R22

Applicable to

Master of Technology
(M. Tech)
Regular Two-Year Degree Programme

(For the Batches admitted from the Academic Year 2022- 2023)

J.B. INSTITUTE OF ENGINEERING AND TECHNOLOGY

(UGC AUTONOMOUS)

Bhaskar Nagar, Yenkapally (V), Moinabad (M), Hyderabad – 500075, Telangana, India

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Offered under **Choice Based Credit System (CBCS)**

1.0 Post-Graduate Degree Programmes in Engineering & Technology (PGP in E & T)

J. B. Institute of Engineering and Technology (JBIET) offers Two Years (Four Semesters) full-time Master of Technology (M. Tech.) Degree programmes, under Choice Based Credit System (CBCS) in the following branches of Engineering and Technology with different specializations as mentioned below:

Computer Science & Engineering	Computer Science & Engineering
Electronics & Communication Engineering	VLSI System Design
Electrical & Electronics Engineering	Electrical Power Systems
Mechanical Engineering	CAD / CAM
Civil Engineering	Structural Engineering

2.0 Eligibility for Admissions

2.1 Admission to the PGPs shall be made subject to eligibility, qualification and specializations prescribed by the University from time to time, for each specialization under each M.Tech programme.

2.2 Admission to the post graduate programme shall be made on the basis of either the merit rank or Percentile obtained by the qualified student in the relevant qualifying GATE Examination/ the merit rank obtained by the qualified student in an entrance test conducted by Telangana State Government (PGCET) for M.Tech. programmes.

2.3 The medium of instructions for all PG Programmes will be ENGLISH only.

3.0 M.Tech. Programme (PGP in E & T) Structure

3.1 The M.Tech Programmes in E & T of JBIET are of Semester pattern, with Four Semesters consisting of Two academic years, each academic year having Two Semesters (First/Odd and Second/Even Semesters). Each Semester shall be of 22 weeks duration (inclusive of Examinations), with a minimum of 90 instructional

days per Semester.

3.3 UGC/AICTE specified definitions/descriptions are adopted appropriately for various terms and abbreviations used in these PG academic regulations, as listed below:

3.3.1 Semester Scheme

Each Semester shall have 'Continuous Internal Evaluation (CIE)' and 'Semester End Examination (SEE)'. Choice Based Credit System (CBCS) and Credit Based Semester System (CBSS) are taken as 'references' for the present set of Regulations. The terms 'SUBJECT' and 'COURSE' imply the same meaning here and refer to 'Theory Subject', or 'Lab Course', or 'Seminar', or 'Comprehensive Viva', or 'Project' as the case may be.

3.3.2 Credit Courses

All subjects / courses are to be registered by the student in a semester to earn credits which shall be assigned to each subject/course in an L: T: P: C (Lecture Periods: Tutorial Periods: Practical Periods: Credits) structure based on the following general pattern:

- One credit for one hour/week/semester for theory/lecture (L) courses
- One credit for two hours/ week/semester for laboratory/ practical (P) courses or tutorials
- Other student activities like study tour, guest lecture, conference/workshop participations, technical paper presentations, and identified mandatory courses, if any, will not carry credits.

3.3.3 Mandatory Courses: A student shall register for all mandatory courses mentioned in the curriculum and get minimum pass marks (i.e., 40% of total marks through internal evaluation only) to get the degree. Grade points obtained in these courses will not be considered for awarding class.

3.3.4 Subject Course Classification

All subjects / courses offered for the Post-Graduate Programme in E & T (M.Tech Degree Programme) are broadly classified as follows. The institute has followed in general the guidelines issued by AICTE/UGC.

S. No	Broad Course Classification	Course Group/Category	Course Description
1	Core Courses (CoC)	PC – Professional Core	Includes subjects related to the parent discipline / department/ Branch of Engineering
		Project Work	M. Tech Project or PG Project or Major Project
		Seminar, Technical paper writing	Seminar/Colloquium based on core contents related to parent discipline/department/ Branch of Engineering
		Comprehensive Viva-Voce	Viva-voce covering all the PG subjects studied during the course work and related aspects
2	Elective Courses (EIE)	PE – Program Electives	Includes elective subjects related to the parent discipline/ department/ Branch of Engineering
		OE - Open Electives	Elective subjects which include inter- disciplinary subjects or subjects in an area outside the parent discipline/department/ Branch of Engineering
Total number of Credits = 68			

4.0. Course Registration

4.1 A 'Faculty Advisor or Counselor' shall be assigned to each specialization, who will advise on the Post Graduate Programme (PGP), its Course Structure and Curriculum, Choice/Option for Subjects/ Courses, based on his competence, progress, pre-requisites and interest.

4.2 The Department invites 'Registration Forms' from students. Registration requests for any 'CURRENT SEMESTER' shall be completed BEFORE the commencement of SEEs (Semester End Examinations) of the 'PRECEDING SEMESTER'.

4.3 A Student can apply for Registration, ONLY AFTER obtaining the 'WRITTEN APPROVAL' from his Faculty Advisor, which should be submitted to the Department

4.4 If the Student submits ambiguous choices or multiple options or erroneous entries during Registration for the Subject(s) / Course(s) under a given/ specified Course Group/ Category as listed in the Course Structure, only the first mentioned Subject/ Course in that Category will be taken into consideration.

4.5 Subject/ Course Options exercised through Registration are final and CANNOT be changed, nor can they be inter-changed; further, alternate choices also will not be considered. However, if the Subject/ Course that has already been listed for Registration by the Department in a Semester could not be offered due to unforeseen or unexpected reasons, then the Student will be allowed to have alternate choice either for a new Subject, if it is offered, or for another existing Subject (subject to availability of seats). Such alternate arrangements will be made by the Head of Department, with due notification and time-framed schedule, within the FIRST WEEK from the commencement of Class-work for that Semester.

4.6 Program electives: The students have to choose 5 Program electives (PE-I to V) from the list of program electives given. (2 PEs in I Semester, 2 PEs in II Semester and 1 in III Semester).

4.7 Open electives: The students have to choose one open elective (OE-I) from the list of open electives given in II year I semester.

5.0 Attendance Requirements

The programmes are offered on the basis of a unit system with each subject being considered a unit.

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5.1 A student is eligible to appear for the semester end examinations, if the student acquires a minimum of 75% of attendance in aggregate of all the subjects / courses (excluding attendance in mandatory courses) for that semester..

5.2 Shortage of attendance in aggregate up to 10% (65% and above, and below 75%) in each semester may be condoned on medical grounds.

5.3 Shortage of attendance below 65% in aggregate shall in no case be condoned.

5.4 Students whose shortage of attendance is not condoned in any semester are not eligible to take their end examinations of that semester.

5.5 A student fulfills the attendance requirement in the present semester, shall not be eligible for readmission into the same class.

5.6 A prescribed fee per subject shall be payable for condoning shortage of attendance.

6.0 Academic Requirements

The following academic requirements have to be satisfied, in addition to the attendance requirements mentioned in item no. 5. The performance of the candidate in each semester shall be evaluated subject-wise, with a maximum of 100 marks per subject / course (theory / practical), on the basis of Internal Evaluation and Semester End Examination.

6.1 A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/course, if he secures not less than 40% of marks (24 out of 60 marks) in the End Semester Examination, and a minimum of 50% of marks (50 out of 100 marks) in the sum total of CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

6.2 A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to a subject/ course, if he secures not less than 50% of the total marks. The student is deemed to have failed, if he (i) does not attend the comprehensive viva-voce as per the schedule given, or (ii) does not present the seminar as required, or (iii) does not present the Technical Paper Writing as required. In such a case, he may reappear for comprehensive viva-voce in supplementary examinations and for seminar/ technical paper writing, in the subsequent semesters, as and when scheduled.

6.3 A student shall register for all subjects for total of 68 credits as specified and listed in the course structure for the chosen specialization, put in required the attendance and fulfill the academic requirements for securing 68 credits obtaining

a minimum of 'B' Grade or above in each subject, and all 68 credits securing Semester Grade Point Average (SGPA) 6.0 (in each semester) and final Cumulative Grade Point Average (CGPA) (i.e., CGPA at the end of PGP) 6.0, to complete the PGP successfully.

6.4 Marks and Letter Grades obtained in all those subjects covering the above specified 68 credits alone shall be considered for the calculation of final CGPA, which will be indicated in the Grade Card /Marks Memo of second year second semester.

6.5 If a student registers for extra subject(s) (in the parent department or other departments/ branches of Engineering) other than those listed subjects totalling to 68 credits as specified in the course structure, the performance in extra subject(s) (although evaluated and graded using the same procedure as that of the required 68 credits) will not be taken into account while calculating the SGPA and CGPA. For such extra subject(s) registered, a certificate will be issued with a letter grade indicated as a performance measure, subject to completion of the attendance and academic requirements as stated in items 5 and 6.1 - 6.3.

6.6 A student eligible to appear for the Semester End Examination in any subject, but absent from it or failed (failing to secure 'B' Grade or above), may reappear for that subject at the supplementary examination as and when conducted. In such cases, his Internal Marks assessed earlier for that subject will be carried over, and added to the marks secured in the supplementary examination, for the purpose of evaluating his performance in that subject.

6.7 A Student who fails to earn 68 credits as per the specified course structure, and as indicated above, within four academic years from the date of commencement of his first year first semester, shall forfeit his seat in M.Tech. programme and his admission shall stand cancelled.

7.0 Evaluation - Distribution and Weightage of Marks

7.1 The performance of a student in every subject/course (including practicals) will be evaluated for 100 marks each, with 40 marks allotted for Continuous Internal Evaluation (CIE) and 60 marks for Semester End Examination (SEE).

7.2 For theory courses, during the semester there is **2 mid-term** examinations (internal exams of **30 marks** each) and **2 assignments** carrying **10 marks** each.

7.3 Each mid-term examination will be of 1 hour 20 minutes consisting of Part-A (short

answer questions) for **10 marks** and Part-B (long answer) for **20 marks**. Part-A consists of Five two marks questions and Part- B consists of five questions carrying 5 marks each and student should answer 4 questions.

7.4 First mid-term examination is conducted from first 2 Modules of syllabus and second mid-term examination is conducted for remaining 3 Modules of syllabus during the last week of instruction.

7.5 The Continuous Internal Evaluation for theory course shall be made as average of marks obtained in CIE – I and CIE –II as detailed in the table below.

CIE – I	Marks	CIE - II	Marks
MID – I	30	MID - II	30
Assignment – I	10	Assignment - II	10
Total	40	Total	40

7.6 If a student is absent for any test/assignment, he is awarded zero marks for that test/assignment. However, a candidate may be permitted on genuine grounds provided he/she has taken permission before the mid-term examination from the Head of the Department. Moreover, he/she has to apply for makeup examinations within a week after completion of mid-term examinations. A subcommittee will be constituted with the following composition to look into such cases.

Subcommittee-composition:

S. No.	Faculty Member	Designation
1	Concern Head of the Department	Chairman
2	Senior faculty nominated by Principal	Member
3	One Senior faculty member of the concern department	Member
4	One faculty member of the other department	Member
5	Additional Controller of Examinations	Member

7.7 The details of the Question Paper pattern for Semester End Examination (Theory) are given below:

The Semester End Examination will be conducted for **60 marks**. It consists of two parts. i).Part A for **10 marks**, ii). Part B for **50 marks**.

- Part-A is a compulsory question which consists of ten sub-questions from all units carrying equal marks.
- Part-B consists of five questions carrying **10 marks** each. Each of these questions is from one unit and may contain sub-questions. For each question there will be an "either" "or" choice, which means that there will be two questions from each unit and the student should answer either of the two questions.

7.8 For practical subjects, **60 marks** shall be awarded for performance in the Semester End Examinations and **40 marks** shall be awarded as Internal Marks. Out of the **40 marks** for internal evaluation, day-to-day work in the laboratory is evaluated for **30 marks** and internal practical examination is evaluated for **10 marks** conducted by the laboratory teacher concerned.

The semester end examination is conducted with an external examiner and the laboratory teacher. The external examiner is selected and appointed by the Principal from the list submitted by Head of the Department

7.9 The semester end examination is conducted with an external examiner and the laboratory teacher. The external examiner is selected and appointed by the Principal from the list submitted by Head of the Department.

7.10 There shall be a Seminar presentation during II Year I semester. For Seminar student under the supervision of a faculty member shall collect literature on a topic and critically review the literature and submit a report to the Department. Upon acceptance of the report by the Department committee candidate shall make an oral presentation before the Department Commitee. The Department Committee comprising of Head of The Department, supervisor, and two other senior faculty members of the Department shall evaluate for 50 marks. There is no external Evaluation for the Seminar.

7.11 There shall be a mini project preferably suggested by the industry of their specialization. The mini project shall be carried out during the summer vacation between I Year II Semester and II year I Semester is evaluated for 50 marks in the II Year I Semester by the Head, Supervisor/ mentor and a senior faculty of the department. A candidate has to secure a minimum of 50% of marks (25 out of 50) to be declared successful. If he fails to obtain the minimum marks, he has to reappear for the same during the supplementary examinations as and when conducted, subject to item 3.2.

7.12 There shall be a dissertation/major project work of one-year duration which contributes strong weightage in the curriculum in the II year. It is expected to undertake industrially relevant problem to develop an optimal solution through extensive research work. The students and faculty can design the research project in consultation with industry preferably in the region. The planning of laboratory work/modelling/computational work with execution schedule is suggested at the beginning of the programme to ensure expected outcome. This will lead to creation of patents from the result of the programme.

7.13 Every candidate shall be required to submit a thesis or dissertation on a topic approved by the Project Review Committee.

7.14 A Project Review Committee (PRC) shall be constituted with the Head of the Department as Chairperson, Project Coordinator and one senior faculty member of the Departments offering the M. Tech. programme.

7.15 Registration of Project Work: A candidate is permitted to register for the project work after satisfying the attendance requirement in all the subjects, both theory and practicals.

7.16 After satisfying 7.15, a candidate has to present in Project Work Review I, in consultation with his Project Supervisor, the title, objective and plan of action of his project work to then Project Work Review Committee (PRC) for approval within four weeks from the commencement of Second Year First Semester. Only after obtaining the approval of the PRC can the student initiate the Project work.

7.17 If a candidate wishes to change his supervisor or topic of the project, he can do so with the approval of the PRC. However, the PRC shall examine whether or not the change of topic/supervisor leads to a major change of his initial plans of project proposal. If yes, his date of registration for the project work starts from the date of change of Supervisor or topic as the case may be.

7.18 A candidate is permitted to submit Project Thesis only after successful completion of all theory and practical courses with the approval of PRC not earlier than 40 weeks from the date of approval of the project work. For the approval of PRC the candidate shall submit the draft copy of thesis to the Head of the Department and make an oral presentation before the PRC.

7.19 The major project work shall be carried out in two stages: Project Stage – I during II Year I Semester, Project Stage – II during II Year II Semester. Each stage will be evaluated for 100 marks. Student has to submit project work report at the end of each semester. First report includes project work carried out in II Year I semester and second report includes project work carried out in II Year I & II Semesters. SEE for both project stages shall be completed before the commencement of SEE Theory examinations.

7.20 For Project Stage – I, the Project Review Committee shall evaluate the project work for 50 marks and project supervisor shall evaluate for 50 marks. The student is deemed to have failed, if he (i) does not submit a report on Project Stage - I or does not make a presentation of the same before the evaluation committee as per schedule, or (ii) secures less than 50% marks in the sum total of the CIE and SEE taken together. A student who has failed may reappear once for the above evaluation, when it is scheduled again; if he fails in such 'one reappearance' evaluation also, he has to reappear for the same in the next subsequent semester, as and when it is scheduled.

7.21 For Project Stage – II, the external examiner shall evaluate the project work for 50 marks and the project supervisor shall evaluate it for 50 marks. The student is deemed to have failed, if he (i) does not submit a report on Project Stage - II, or does not make a presentation of the same before the external examiner as per schedule, or (ii) secures less than 50% marks in the sum total of the CIE and SEE taken together. For conducting viva-voce of project stage – II, Principal selects an external examiner from the panel of experts in the relevant branch submitted by the HOD.

A student who has failed may reappear once for the above evaluation, when it is scheduled again; if student fails in such 'one reappearance' evaluation also, he has to reappear for the same in the next subsequent semester, as and when it is scheduled.

7.22 After approval from the PRC, the soft copy of the thesis should be submiitted to the Department for ANTI-PLAGIARISM for the quality check and the plagiarism report should be included in the final thesis. If the copied information is less than 30%, then only thesis will be accepted for submission.

7.23 Three copies of the Project Thesis certified by the supervisor shall be submitted to the College, after submission of a research paper related to the project work in a UGC approved journal. A copy of the submitted research paper shall be attached to thesis.

7.24 The Project Viva-Voce External examination marks must be submitted to the Exam Branch on the same day of the examination.

8.0 Re-Admission/Re-Registration

8.1 Re-Admission for Discontinued Student

A student, who has discontinued the M.Tech. degree programme due to any reason whatsoever, may be considered for 'readmission' into the same degree programme (with the same specialization) with the academic regulations of the batch into which he gets readmitted, with prior permission from the authorities concerned, subject to item 6.6.

9.0 Examinations and Assessment - The Grading System

9.1 Grades will be awarded to indicate the performance of each student in each Theory Subject, or Lab/Practicals, or Seminar, or Technical Paper Writing or Project, etc., based on the % of marks obtained in CIE + SEE (Continuous Internal Evaluation + Semester End Examination, both taken together) as specified in Item 7 above, and a corresponding Letter Grade shall be given.

9.2 As a measure of the student's performance, a 10-point Absolute Grading System using the following Letter Grades (UGC Guidelines) and corresponding percentage of marks shall be followed:

% of Marks Secured in a Subject/Course (Class Intervals)	Letter Grade (UGC Guidelines)	Grade Points
Greater than or equal to 90%	O (Outstanding)	10
80 and less than 90%	A+ (Excellent)	9
70 and less than 80%	A (Very Good)	8
60 and less than 70%	B+ (Good)	7
50 and less than 60%	B (Above Average)	6
Below 50%	F (FAIL)	0
Absent	Ab	0

9.3 A student obtaining F Grade in any Subject is deemed to have 'failed' and is required to reappear as 'Supplementary Candidate' for the Semester End Examination (SEE), as and when conducted. In such cases, his Internal Marks (CIE Marks) in those subjects will remain as obtained earlier.

9.4 If a student has not appeared for the examinations, 'Ab' Grade will be allocated to him for any subject and shall be considered 'failed' and will be required to reappear as 'Supplementary Candidate' for the Semester End Examination (SEE), as and when conducted.

9.5 A Letter Grade does not imply any specific marks percentage; it is only the range of percentage of marks.

9.6 In general, a student shall not be permitted to repeat any Subject/ Course (s) only for the sake of 'Grade Improvement' or 'SGPA/ CGPA Improvement'.

9.7 A student earns Grade Point (GP) in each Subject/ Course, on the basis of the Letter Grade obtained by him in that Subject/ Course. The corresponding 'Credit Points' (CP) are computed by multiplying the Grade Point with Credits for that particular Subject/ Course.

Credit Points (CP) = Grade Point (GP) x Credits …. For a Course

9.8 The student passes the Subject/ Course only when he gets GP ≥ 6 (B Grade or above).

9.9 The Semester Grade Point Average (SGPA) is calculated by dividing the Sum of Credit Points (CP) secured from ALL Subjects/ Courses registered in a Semester, by the Total Number of Credits registered during that Semester. SGPA is rounded off to TWO Decimal Places. SGPA is thus computed as

$$SGPA = \frac{\sum_{i=1}^{N} C_i G_i}{\sum_{i=1}^{N} Ci} \text{ for each Semester}$$

where 'i' is the subject indicator index (takes into account all subjects in a semester), 'N' is the no. of subjects 'registered' for the semester (as specifically required and listed under the course structure of the department), C_i is the no. of credits allotted to the i^{th} subject, and G_i represents the grade points (GP) corresponding to the letter grade awarded for that i^{th} subject.

9.10 The Cumulative Grade Point Average (CGPA) is a measure of the overall cumulative performance of a student over all Semesters considered for registration. The CGPA is the ratio of the Total Credit Points secured by a student in ALL registered Courses in ALL Semesters, and the Total Number of Credits registered in ALL the Semesters. CGPA is rounded off to TWO Decimal Places. CGPA is thus computed from the I Year Second Semester onwards, at the end of each Semester, as per the formula

$$\text{CGPA} = \left\{ \frac{\sum_{J=1}^{M} C_J G_J}{\sum_{J=1}^{N} C_J} \right\} \text{..... FOR ALL "S" SEMESTERS REGISTERED}$$

(I.E., UP TO AND INCLUSIVE OF S SEMESTER, S ≥ 2),

where 'M' is the TOTAL no. of Subjects (as specifically required and listed under the Course Structure of the parent Department) the Student has 'REGISTERED' for from the 1^{st} Semester onwards up to and inclusive of the Semester S (obviously M > N), 'j' is the Subject indicator index (taking into account all Subjects from 1 to S Semesters), C_i is the no. of Credits allotted to the j^{th} Subject, and C_i represents the Grade Points (GP) corresponding to the Letter Grade awarded for that j^{th} Subject. After registration and completion of I Year I Semester however, the SGPA of that Semester itself may be taken as the CGPA, as there are no cumulative effects.

Illustration of calculation of SGPA:

Course/Subject	Credits	Letter Grade	Grade Points	Credit Points
Course 1	4	A	8	4 x 8 = 32
Course 2	4	O	10	4 x 10 = 40
Course 3	4	C	5	4 x 5 = 20
Course 4	3	B	6	3 x 6 = 18
Course 5	3	A+	9	3 x 9 = 27
Course 6	3	C	5	3 x 5 = 15
	21			152

$$SGPA = \frac{152}{21} = 7.24$$

Illustration of calculation of CGPA:

Semester	Credits	SGPA	Credits*SGPA
Semester-I	16	7	16 x 7 = 112
Semester-II	18	6	18 x 6 = 108
Semester-III	18	6.5	18x 6.5 = 117
Semester-IV	16	6	16 x 6 = 96
	68		433

$$CGPA = \frac{433}{68} = 6.37$$

10.0 Award of Degree and Class

10.1 If a student who registers for all the specified Subjects/ Courses as listed in the Course Structure, satisfies all the Course Requirements, and passes the examinations prescribed in the entire PG Programme (PGP), and secures the required number of 68 Credits (with CGPA 6.0), shall be declared to have 'QUALIFIED' for the award of the M.Tech. Degree in the chosen Branch of Engineering and Technology with the specialization that he was admitted into.

10.2 Award of Class

After a student has earned the requirements prescribed for the completion of the programme and is eligible for the award of M.Tech. Degree, he shall be placed in one of the following three classes based on the CGPA:

Class Awarded	CGPA
First Class with Distinction	≥ 7.75
First Class	6.75≤ CGPA < 7.75
Second Class	6.00≤ CGPA < 6.75

A student with final CGPA (at the end of the **PGP) < 6.00** shall not be eligible for the Award of Degree.

11.0 Withholding of Results

If the student has not paid the dues, if any, to the Institution or if any case of indiscipline is pending against him, the result of the student will be withheld and he will not be allowed into the next semester.

12.0. Transitory Regulations

12.1 A student who has been detained in any semester of I Year of Previous Regulations due to lack of attendance, shall be permitted to join the same semester of I Year of R22 Regulations and he is required to complete the study of M.Tech programme within the stipulated period of four academic years from the date of first admission in I Year I semester. The R22 Academic Regulations under which a student has been readmitted shall be applicable to that student from that semester.

12.2 For student readmitted to R22 Regulations, the maximum credits that a student acquires for the award of the degree, shall be the sum of the total number of credits secured in previous regulations of his/her study including R22 Regulations.

12.3 If a student readmitted to R22 Regulations, has any subject with 80% of syllabus common with his/her previous regulations, that particular subject in R22 regulations will be substituted by another subject to be suggested by the Concerned Board Of Studies (BOS).

13 General

13.1 The academic regulation should be read as a whole for the purpose of any interpretation.

13.2 In case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Institution is final.

13.3 The Institution may change or amend the academic regulations or syllabi at any time and the changes or amendments made shall be applicable to all the students with effect from the dates notified by the Institution.

MALPRACTICES RULES

DISCIPLINARY ACTION FOR / IMPROPER CONDUCT IN EXAMINATIONS

	Nature of Malpractices/Improper conduct	Punishment
	If the student:	
1.(a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which student is appearing but has not made use of (material shall include any marks on the body of the student which can be used as an aid in the subject of the examination)	Expulsion from the examination hall and cancellation of the performance in that subject only.
(b)	Gives assistance or guidance or receives it from any other student orally or by any other body language methods or communicates through cell phones with any student or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the students involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2.	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the student is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the student has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year.

3.	Impersonates any other student in connection with the examination.	The student who has impersonated shall be expelled from examination hall. The student is also debarred and forfeits the seat. The performance of the original student who has been impersonated, shall be cancelled in all the subjects of the examination (including practicals and project work) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester/year. The student is also debarred for two consecutive semesters from class work and all End examinations. The continuation of the course by the student is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.
4.	Smuggles in the answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the student has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The student is also debarred for two consecutive semesters from class work and all End examinations. The continuation of the course by the student is subject to the academic regulations in connection with forfeiture of seat.
5.	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that subject.

6.	Refuses to obey the orders of the chief superintendent /assistant superintendent / any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in charge or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer-in-charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the college campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	In case of students of the college, they shall be expelled from examination halls and cancellation of their performancein that subject and all other subjects the student(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The students also are debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.
7.	Leaves the exam hall taking away answer script or intentionally tears off the script or any part there of inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the student has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The student is also debarred for two consecutive semesters from class work and all End examinations. The continuation of the course by the student is subject to the academic regulations in connection with forfeiture of seat.

8.	Possesses any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the student has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The student is also debarred and forfeits the seat.
9.	If student of the college, who is not a student for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the student has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The student is also debarred and forfeits the seat. Person(s) who do not belong to the college will be handed over to the police and, a police case will be registered against them.
10.	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the student has already appeared for including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year.
11.	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other subjects the student has appeared for including practical examinations and project work of that semester/year examinations.
12.	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the Examination Result Processing Committee (ERPC) for further action to award a suitable punishment.	

JBIET-R22	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech

M.Tech. (VLSI SYSTEM DESIGN)
Course Structure

I YEAR I SEMESTER

S. No	Code	Course Title	L	T	P/D	Credits
1	LM61A	Digital System Design	3	0	0	3
2	LM61B	Digital CMOS Integrated Circuit Design	3	0	0	3
3	LM61C LM61D LM61E	1. Scripting Languages for VLSI 2. Digital System Design using HDL 3. Microcontrollers and Programmable Digital Signal Processors	3	0	0	3
4	LM61F LM61G LM61H	1. CPLD and FPGA Architectures and Applications 2. Nano materials and Nanotechnology 3. IOT and its Applications	3	0	0	3
5	LM61I	HDL Simulation Lab	0	0	4	2
6	LM61J	Digital CMOS IC Design Lab	0	0	4	2
7	LM91A	Soft Skills	2	0	0	0
Total			**14**	**0**	**8**	**16**

I YEAR II SEMESTER

S. No	Code	Course Title	L	T	P/D	Credits
1	LM62A	Analog CMOS IC Design	3	0	0	3
2	LM62B	Low Power VLSI Design	3	0	0	3
3	LM62C LM62D LM62E	1. VLSI Signal Processing 2. RF IC Architecture 3. SOC Design	3	0	0	3
4	LM62F LM62G LM62H	1. Hardware Software Co-Design 2. Image and Video Processing 3. Design for Testability	3	0	0	3
5	LM92A	Research Methodology and IPR	2	0	0	2
6	LM62I	Analog CMOS IC Design Lab	0	0	4	2
7	LM62J	VLSI Design and Verification Lab	0	0	4	2
8	LM92B	Personality Development and Professional values	2	0	0	0
Total			**16**	**0**	**8**	**18**

JBIET-R22	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech
M.Tech. (VLSI SYSTEM DESIGN) Course Structure		

II YEAR –I SEMESTER

S. No.	Code	Course Title	L	T	P	Credits
1	LM63A LM63B LM63C	1.Memory Technologies 2.CAD for VLSI 3.Artificial Intelligence	3	0	0	3
2		Open Elective	3	0	0	3
3	LM63D	Mini Project	0	0	4	2
4	LM63E	Technical Seminar	0	0	2	1
5	LM63F	Phase-I Dissertation	0	0	18	9
Total			6	0	24	18

II YEAR – II SEMESTER

S. No.	Code	Course Title	L	T	P	Credits
1	LM64A	Phase-II Dissertation	0	0	32	16
Total			**0**	**0**	**32**	**16**

AY 2022-23 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD I Year – I Sem			
Course Code: LM61A	**DIGITAL SYSTEM DESIGN**	**L**	**T**	**P**	**D**
Credits: 3		**3**	**0**	**0**	**0**

Pre-requisite: Digital Electronics

Course Objectives:

1. To design the Finite State Model.
2. To design ROMs, PALs and PLAs and Adders.
3. To Realize SM Chart and implement Binary Multiplier.
4. To understand Fault detection and diagnose faults by conventional methods.
5. To understand different Fault diagnosis approaches.

Module 1

Unit-1: Minimization and Transformation of Sequential Machines

The Finite State Model – Capabilities and limitations of FSM – State equivalence and machine minimization – Simplification of incompletely specified machines.

Unit-2: Fundamental mode model

Flow table – State reduction – Minimal closed covers – Races, Cycles and Hazards.

Module 2

Unit-1: Digital Design

Digital Design using ROMs, PALs and PLAs, BCD adder, 32 – bit adder, State graphs for control circuits, Scoreboard and Controller, A shift and add multiplier, Array multiplier, Keypad Scanner, Binary divider.

Module 3

Unit-1: SM Charts

State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of Binary Multiplier, dice game controller.

Module 4

Unit-1: Fault Modeling & Test Pattern Generation

Logic Fault model – Fault detection & Redundancy- Fault equivalence and fault location –Fault dominance – Single stuck at fault model – Multiple stuck at fault models –Bridging fault model.

Unit-2: Fault diagnosis of combinational circuits

Fault diagnosis by conventional methods – Path sensitization techniques, Boolean Difference

method – Kohavi algorithm – Test algorithms – D algorithm, PODEM, Random testing, Transition count testing, Signature analysis and test bridging faults.

Module 5

Unit-1: Fault Diagnosis in Sequential Circuits

Circuit Test Approach, Transition Check Approach – State identification and fault detection experiment, Machine identification, Design of fault detection experiment.

Text Books:

1. Fundamentals of Logic Design – Charles H. Roth, 5th Ed., Cengage Learning.
2. Digital Systems Testing and Testable Design – Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman- John Wiley & Sons Inc.
3. Logic Design Theory – N. N. Biswas, PH.

Reference Books:

1. Switching and Finite Automata Theory – Z. Kohavi , 2nd Ed., 2001, TMH.
2. Digital Design – Morris Mano, M.D. Ciletti, 4th Edition, PHI.
3. Digital Circuits and Logic Design – Samuel C. Lee , PHI.

E- Resources:

1. http://nptel.ac.in/downloads
2. https://www.youtube.com/watch?v=CL3ups78jrs
3. http://www.nptelvideos.in/2012/12/digital-systems-design.html

Course Outcomes:

At the end of the course, students will be able to

1. design the Finite State Model.
2. design ROMs, PALs and PLAs and Adders.
3. realize SM Chart and implement Binary Multiplier.
4. understand Fault detection and diagnose faults by conventional methods.
5. understand different Fault diagnosis approaches.

AY 2022-23 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD I Year – I Sem			
Course Code: LM61B	**DIGITAL CMOS INTEGRATED CIRCUIT DESIGN**	**L**	**T**	**P**	**D**
Credits: 3		**3**	**0**	**0**	**0**

Pre-requisite: IC Technologies, Digital Electronics.

Course Objectives:

1. To describe over view about evolution of CMOS integrated circuits.
2. To provide knowledge about Combinational and Sequential MOS logic circuits.
3. To introduce and familiarize with the various logic circuits.
4. To prepare them to face the challenges in dynamic logic circuits.
5. To create interest in the integrated circuit design and prepare them to face the challenges in VLSI technology

Module 1

Unit-1: MOS Design

Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

Module 2

Unit-1: Combinational MOS Logic Circuits

MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates, AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

Module 3

Unit-1: Sequential MOS Logic Circuits

Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flipflop.

Module 4

Unit-1: Dynamic Logic Circuits

Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

Module 5

Unit-1: Semiconductor Memories

Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation, Leakage currents in SRAM cells, Flash Memory- NOR flash and NAND flash.

Text Books:

1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

References Books:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011.
2. Digital Integrated Circuits–A Design Perspective, Jan M.Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2nd Ed., PHI Vranesis, TMH, 2nd edition 2010.
3. Digital Logic Design using Verilog, State machine & synthesis for FPGA, Sunggulee, Cengage Learning, 2009.
4. Verilog HDL- SamirPalnitkar, 2nd edition.
5. Advanced Digital Design with Verilog HDL- Michael D. Ciletti, PHI, 2005.
6. Digital Systems Design using VHDL- Charles H Roth, Jr. Thomson Publications, 2004.

E - Resources:

1. http://nptel.ac.in/downloads
2. https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/6-374-analysis-and-design-of-digital-integrated-circuits-fall-2003/lecture-notes/
3. https://nptel.ac.in/courses/108/106/108106069/

Course Outcomes:

At the end of the course, students will be able to

1. know about the various Combinational and Sequential MOS logic circuits.
2. gain in-depth knowledge of applying the concepts on real time applications
3. understand the design of dynamic MOS logic circuits.
4. illustrate the design of semiconductor memories.
5. understand the basic concepts of Boolean expressions.

AY 2022-23 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD I Year – I Sem			
Course Code: LM61C	**SCRIPTING LANGUAGES FOR VLSI (Program Elective-I)**	**L**	**T**	**P**	**D**
Credits: 3		**3**	**0**	**0**	**0**

Pre-requisite: Introduction to PERL

Course Objectives:

1. To describe the need of using scripting language programs.
2. To use PERL scripting language at the instances required.
3. To apply advanced level PERL for software automation.
4. To employ the PERL scripting language for file system navigation.
5. To illustrate software automation using TCL.

Module 1

Unit-1: Introduction to Scripts and Scripting

Characteristics and uses of scripting languages, Introduction to PERL, Names and values, Variables and assignment, Scalar expressions, Control structures, Built-in functions, Collections of Data.

Unit-2: Working with arrays and subroutines

Working with arrays, Lists and hashes, Simple input and output, Strings, Patterns and regular expressions, Subroutines, Scripts with arguments.

Module 2

Unit-1: Advanced PERL

Finer points of Looping, Subroutines, Using Pack and Unpack, Working with files, Navigating the file system, Type globs, Eval, References, Data structures, Packages, Libraries and modules.

Unit-2: Objects and modules

Objects, Objects and modules in action, Tied variables, Interfacing to the operating systems, Security issues.

Module 3

Unit-1: TCL

The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow, Data structures, Simple input/output, Procedures, Working with Strings, Patterns, Files and Pipes, Example code.

Module 4

Unit-1: Advanced TCL

The eval, source, exec and up-level commands, Libraries and packages, Namespaces, Trapping errors, Event-driven programs, Making applications 'Internet-aware', 'Nuts-and-bolts' internet programming,

Unit-2: Security Issues

Security issues, running untrusted code, The C interface.

Module 5

Unit-1: TK and JavaScript

Visual tool kits, Fundamental concepts of TK, TK by example, Events and bindings, Geometry managers, PERL-TK. JavaScript – Object models, Design Philosophy, Versions of JavaScript, The Java Script core language, Basic concepts of Python.

Unit-2: Object Oriented Programming Concepts (Qualitative Concepts Only)

Objects, Classes, Encapsulation, Data Hierarchy.

Text Books:

1. The World of Scripting Languages- David Barron, Wiley Student Edition, 2010.
2. Practical Programming in Tcl and Tk - Brent Welch, Ken Jones and Jeff Hobbs.,Fourth edition.
3. Java the Complete Reference - Herbert Schildt, 7th Edition, TMH.

Reference Books:

1. Tcl/Tk: A Developer's Guide- Clif Flynt, 2003, Morgan Kaufmann Series.
2. Tcl and the Tk Toolkit- John Ousterhout, 2nd Edition, 2009, Kindel Edition.

E - Resources:

1. https://nptel.ac.in/courses/117/106/117106113/
2. https://nptel.ac.in/courses/106/105/106105084/
3. youtube.com/watch?v=Avdp-Uj3Qyc
4. https://www.perltutorial.org/

Course Outcomes:

On completion of the course, the students will be able to

1. be in a position to judge whether scripting language program is needed for a particular code.
2. acquainted with the basic level scripting language programming in PERL.
3. be skillful to code in PERL for advanced level software automation.
4. have the programming skills to automate the software for event-driven programs too.
5. be in a position to demonstrate software automation using Java Script, Perl-TK and in basic level using python scripting language.

AY 2022-23 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD I Year – I Sem			
Course Code: LM61D	DIGITAL SYSTEM DESIGN USING HDL (Program Elective-I)	L	T	P	D
Credits: 3		3	0	0	0

Pre-requisite: VLSI and Digital Electronics.

Course Objectives: The Student will

1. learn digital design of Sequential Machines.
2. understand drawing state graphs.
3. understand realization and implementation of SM Charts.
4. analyse fault modeling and test pattern generation of Combinational circuits.
5. apply fault diagnosis in sequential circuits and understand machine design, identification of fault detection experiment.

Module 1

Unit-1: Digital System Design Automation and RTL Design with Verilog

Digital Design Flow-design entry, Test bench in Verilog, Design validation, Compilation and synthesis, Post synthesis simulation, Timing analysis, Hardware generation in Verilog, Test Benches.

Module 2

Unit-1: Verilog Language Concepts

Characterizing Hardware Languages, Module Basics, Verilog Simulation Model, Compiler Directives, System Tasks and Functions.

Module 3

Unit-1: Combinational Circuit Description

Module Wires, Gate Level Logic, Hierarchical Structures, Describing Expressions with Assign statements, Behavioral Combinational Descriptions, Combinational Synthesis.

Module 4

Unit-1: Sequential Circuit Description

Sequential models, Basic Memory Components, Functional Registers, State Machine Coding, Sequential Synthesis.

Unit-2: Component Test, Verification and Detailed Modeling

Test Bench, Test Bench Techniques, Design Verification, Assertion Verification, Text Based Test Benches, Detailed Modeling- Switch Level Modeling, Strength Modeling.

Module 5

Unit-1: RTL Design and Test

Sequential Multiplier, Shift-and-Add Multiplication process, Sequential multiplier design, Multiplier testing, Von Neumann Computer Model- Processor and memory model, processor model specification, designing the adding CPU, Design of datapath, Control part design, Adding CPU verilog description, tesing adding CPU.

Text Books:

1. Zainalabdien Navabi, Verlog Digital System Design, TMH, 2nd edition.

References Books:

1. Fundamentals of Digital Logic with Verilog design by Stephen. Brown and Zvonko Vranesis, TMH, 2nd edition 2010.
2. Digital Logic Design using Verilog, State machine & synthesis for FPGA, Sunggulee, Cengage Learning, 2009.
3. Verilog HDL- Samir Palnitkar, 2nd edition.
4. Advanced Digital Design with Verilog HDL- Michael D. Ciletti, PHI, 2005.
5. Digital Systems Design using VHDL- Charles H Roth, Jr. Thomson Publications, 2004.

E - Resources:

1.http://nptel.ac.in/downloads.

Course Outcomes:

After completion of the course, the Student will be able to

1. create understanding of the design techniques of sequential Machines.
2. create understanding of the fundamental concepts of PLD's, design of FPGA's.
3. learn implementation of SM charts in combinational and sequential circuits.
4. develop skills in modeling fault free combinational circuits.
5. develop skills in modeling Sequential circuits in terms of reliability, availability and safety.

AY 2022-23 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD I Year – I Sem			
Course Code: LM61E	MICROCONTROLLERS AND PROGRAMMABLE DIGITAL SIGNAL PROCESSORS (Program Elective -I)	L	T	P	D
Credits: 3		3	0	0	0

Pre-requisite: Microprocessors and Microcontrollers, Digital Signal Processing.

Course Objectives:

1. To make students familiar with the most important ARM processor core based SoC with requirements of embedded applications.
2. To make students aware about the architecture of Programmable DSP Processors.
3. To make students develop small applications by utilizing the ARM processor core and DSP processor.
4. To introduce various techniques of digital signal processing that are fundamental to various industrial applications.
5. To learn the basis of DSP systems, its theory and practical implementation of different kind of algorithms.

Module 1:

Unit-1: ARM Cortex-M3 processor

ARM Cortex-M3 processor: Applications, Programming model – Registers, Operation - modes, Exceptions and Interrupts, Reset Sequence Instruction Set, Unified Assembler Language.

Unit-2: Memory Maps

Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations, Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces.

Module 2:

Unit-1: Vector Tables

Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behaviour, Fault Exceptions, Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller, Basic Configuration.

Unit-2: SYSTICK Timer

SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency.

Module 3:

Unit-1: LPC 17xx microcontroller

LPC 17xx microcontroller- Internal memory, GPIOs, Timers, ADC, UART and other serial interfaces, PWM, RTC, WDT.

Module 4:

Unit-1: Programmable DSP (P-DSP) Processors

Programmable DSP (P-DSP) Processors: Harvard architecture, Multi port memory, architectural structure of P-DSP- MAC unit.

Unit-2: Barrel shifters

Barrel shifters, Introduction to TI DSP processor family.

Module 5:

Unit-1: VLIW architecture

VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths.

Unit-2: C6000 family

Introduction to Instruction level architecture of C6000 family, Assembly Instructions, memory addressing for arithmetic, logical operations.

Text Books:

1.Joseph Yiu, "The definitive guide to ARM Cortex-M3", Elsevier, 2nd Edition.

2.Venkatramani B. and Bhaskar M. "Digital Signal Processors: Architecture, Programming and Applications", TMH, 2nd Edition.

Reference Books

1. Sloss Andrew N, Symes Dominic, Wright Chris, "ARM System Developer's Guide: Designing and Optimizing", Morgan Kaufman Publication.
2. Steve furber, "ARM System-on-Chip Architecture", Pearson Education.
3. Frank Vahid and Tony Givargis, "Embedded System Design", Wiley.

E- Resources

1.https://nptel.ac.in/courses/117/104/117104072/
2.https://nptel.ac.in/content/storage2/courses/108105057/Pdf/Lesson-10.pdf
3. https://nptel.ac.in/courses/106/105/106105193/
4. Technical references and user manuals on www.arm.com, NXP Semiconductor www.nxp.com and Texas Instruments www.ti.com

Course Outcomes:

After completion of the course, the Student will be able to

1. compare and select ARM processor core based SoC and their memory maps.
2. explore the basic configuration of vector tables and SYSTICK Timer.
3. get an in-depth knowledge of LPC 17xx microcontroller and its interfaces.
4. identify and characterize architecture of Programmable DSP Processors.
5. obtain basic concepts of VLIW and C6000 in terms of architecture and operations.

AY 2022-23 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD I Year – I Sem			
Course Code: LM61F	**CPLD AND FPGA ARCHITECURES AND APPLICATIONS (Program Elective-II)**	**L**	**T**	**P**	**D**
Credits: 3		**3**	**0**	**0**	**0**

Pre-requisite: VLSI Technology.

Course Objectives

1. To understand the concept of Programmable Logic Device architectures and technologies.
2. Underlying FPGA architectures and technologies in detail.
3. To understand the difference between CPLDs and FPGAs.
4. To provide knowledge about SRAM Programmable FPGA Device architecture.
5. To comprehend knowledge about Anti-Fuse Programmable FPGA Device architecture.

Module 1

Unit-1: Introduction to Programmable Logic Devices

Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic.

Unit-2: Complex Programmable Logic Devices

Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

Module 2

Unit-1: Field Programmable Gate Arrays

Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications.

Module 3

Unit-1: SRAM Programmable FPGAs

Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures.

Module 4

Unit-1: Anti-Fuse Programmed FPGAs

Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

Module 5

Unit-1: Design Applications

General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

Text Books:

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.
2. Digital Systems Design - Charles H. Roth Jr, Lizy Kurian John, Cengage Learning.

Reference Books:

1. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/Samiha Mourad, Pearson Low Price Edition.
3. Digital Systems Design with FPGAs and CPLDs - Ian Grout, Elsevier, Newnes.
4. FPGA based System Design - Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.

E-Resources:

1. http://nptel.ac.in/downloads

Course Outcomes:

After completion of course, the student will be able to

1. understand the concept of programmable architectures.
2. illustrate the CPLD and FPGA technologies.
3. study and compare the different architectures of CPLDs and FPGAs.
4. have an ability to know the SRAM Technology based FPGAs.
5. have an ability to know the Anti-Fuse Technology based FPGAs.

AY 2022-23 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD I Year – I Sem			
Course Code: LM61G	NANOMATERIALS AND NANOTECHNOLOGY (Program Elective-II)	L	T	P	D
Credits: 3		3	0	0	0

Pre-requisite: Introduction to VLSI and Nanotechnology.

Course Objectives:

The student will

1. understand the basic science behind the design and fabrication of nano scale systems.
2. gain knowledge on fundamentals of Nanomaterials and its dimensions.
3. describe the concepts of MEMS.
4. gain complete knowledge about CNTs.
5. apply the various applications of Nanomaterials and Nanotechnology in various fields.

Module 1

Unit-1: Introduction

Introduction of nano materials and nanotechnologies, Features of nanostructures, Applications of nano materials and technologies.

Unit-2: Nanomaterials Dimension and Structures

Nano Dimensional Materials 0D, 1D, 2D structures – Size Effects – Fraction of Surface Atoms – Specific Surface Energy and Surface Stress – Effect on the Lattice Parameter – Phonon Density of States – the General Methods available for the Synthesis of Nanostructures – precipitative – reactive – hydrothermal/solvo thermal methods – suitability of such methods for scaling – potential uses.

Module 2

Unit-1: Fundamentals of Nanomaterials

Fundamentals of nanomaterials, Classification, Zero-dimensional nanomaterials, One-dimensional nanomaterials, Two-dimensional nanomaterials, Three dimensional nanomaterials.

Unit-2: Applications

Low-Dimensional Nanomaterials and its Applications, Synthesis, Properties and Applications of Low-Dimensional Carbon-Related Nanomaterials.

Module 3

Unit-1: Micro- and Nanolithography Techniques

Micro- and Nanolithography Techniques, Emerging Applications.

Unit-2: Introduction to MEMS

Introduction to Micro Electro Mechanical Systems (MEMS), Advantages and Challenges of MEMS, Fabrication Technologies, Surface Micromachining, Bulk Micromachining, Molding, Introduction to Nano Phonics.

Module 4

Unit-1: Introduction to CNTs

Introduction, Synthesis of CNTs - Arc-discharge, Laser-ablation, Catalytic growth, Growth mechanisms of CNT's - Multi-walled nanotubes, Single-walled nanotubes Optical properties of CNT's, Electrical transport in perfect nanotubes, Synthesis and Applications of CNT's.

Module 5

Unit-1: Ferroelectric Materials

Ferroelectric materials, Coating, Molecular Electronics and Nanoelectronics, Biological and **E**nvironmental, membrane based application, polymer based application.

Text Books:

1. Kenneth J. Klabunde and Ryan M. Richards, "Nanoscale Materials in Chemistry", 2nd edition, John Wiley and Sons, 2009.

2. I Gusev and A A Rempel, "Nanocrystalline Materials", Cambridge International Science Publishing, 1 st Indian edition by Viva Books Pvt. Ltd. 2008.

3. B. S. Murty, P. Shankar, Baldev Raj, B. B. Rath, James Murday, "Nanoscience and Nanotechnology", Tata McGraw Hill Education 2012.

Reference Books:

1. Bharat Bhushan, "Springer Handbook of Nanotechnology", Springer, 3rd edition, 2010.

2. Kamal K. Kar, "Carbon Nanotubes: Synthesis, Characterization and Applications", Research Publishing Services; 1st edition, 2011, ISBN-13: 978-9810863975.

E - Resources:

1. https://www.youtube.com/watch?v=qUEbxTkPIWI
2. https://nptel.ac.in/courses/118/104/118104008/
3. http://home.iitk.ac.in/~kbalani/doc/Nanostructures_and_Nanomaterials.pdf

Course Outcomes:

After completion of the course, the students will be able to

1. understand the basic science behind the design and fabrication of nano scale systems.

2.understand and formulate new engineering solutions for current problems and competing technologies for future applications.

3. illustrate the concepts of MEMS.

4. be able make inter disciplinary projects applicable to wide areas by clearing and fixing the boundaries in system development.

5. gather detailed knowledge of the operation of fabrication and characterization devices to achieve precisely designed systems.

AY 2022-23 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD I Year – I Sem			
Course Code: LM61H	**IOT AND ITS APPLICATIONS (Program Elective-II)**	**L**	**T**	**P**	**D**
Credits: 3		**3**	**0**	**0**	**0**

Pre-requisite: Knowledge of Data Communication with Computer Networking, Web Technology and programming skills.

Course Objectives:

1. Recognize the factors that contributed to the emergence of IOT.
2. To Design and programming of IOT devices and applications in web Technology.
3. Use of real time IOT protocols for communication.
4. Security of IOT device elements can be achieved.
5. Design of an IOT device to work with Advanced applications.

Module 1:

Unit-1: Introduction to Web Technology & IOT

The Internet of Things & web technologies, Time for Convergence, Towards the IoT Universe, Internet of Things Vision, IoT Strategic Research and Innovation directions, IoT Applications, Future Internet Technologies, Infrastructure.

Unit-2: IOT Networks

Networks and Communication, Processes, Data Management, Security, Privacy & Trust, Device Level Energy Issues, IoT Related Standardization, Recommendations on Research Topics, Introduction to Cloud Computing.

Module 2:

Unit-1: Machine to Machine Communication

History of IoT, the Layering concepts, IoT Communication Pattern, M2M to IoT – A Basic Perspective– Introduction, M2M Value Chains, IoT Value Chains, an emerging industrial structure for IoT.

Unit-2: IoT Architecture

M2M to IoT-An Architectural Overview– Building an architecture, Main design principles and needed capabilities, An IoT architecture outline, standards considerations., IoT protocol Architecture.

Module 3

Unit-1: IoT Modelling

IoT Architecture -State of the Art – Introduction, State of the art, Architecture Reference Model- Introduction, Reference Model and architecture, IoT reference Model, IoT Reference Architecture- Introduction.

Unit-2: IoT Deployment Functional View, Information View, Deployment and Operational View, Other Relevant architectural views.

Module 4

Unit-1: IoT for Industry

Future Factory Concepts, Brownfield IoT, Smart Objects, Smart Applications, Four Aspects in your Business to Master IoT, Application in Remote Monitoring & Sensing, Remote Controlling, Performance Analysis 6LoWPAN.

Unit-2: Big Data Analysis

Value Creation from Big Data and Serialization, IoT for Retailing Industry, IoT For Oil and Gas Industry, Opinions on IoT Application and Value for Industry, Home Management, eHealth.

Module 5

Unit-1: Privacy & Security

Internet of Things Privacy, Security and Governance Introduction, Overview of Governance, Privacy and Security Issues,

Unit-2: Advanced IOT Applications

Sensors and sensor Node and interfacing using any Embedded target boards like Raspberry Pi / Intel Galileo/ARM Cortex/ Arduino.

Text Books:

1. Vijay Madisetti and Arshdeep Bahga, "Internet of Things (A Hands-on-Approach)", 1st Edition, VPT, 2014.
2. Francis daCosta, "Rethinking the Internet of Things: A Scalable Approach to Connecting Everything", 1st Edition, Apress Publications, 2013.
3. 6LoWPAN: The Wireless Embedded Internet, Zach Shelby, Carsten Bormann, Wiley.

Reference Books:

1. The Internet of Things: From RFID to the Next-Generation Pervasive Networked Lu Yan, Yan Zhang, Laurence T. Yang, Huansheng Ning.
2. Internet of Things (A Hands-on-Approach),Vijay Madisetti ,Arshdeep Bahga.
3. Designing the Internet of Things,Adrian McEwen (Author), Hakim Cassimally.
4. Data and Computer Communications; By: Stallings, William; Pearson Education Pte. Ltd., Delhi, 6th Edition.
5. Cloud Computing Bible, Barrie Sosinsky, Wiley-India, 2010.
6. Cuno Pfister, "Getting Started with the Internet of Things", O Reilly Media, 2011.
7. Internet of Things: Converging Technologies for Smart Environments and Integrated Ecosystems, Dr. Ovidiu Vermesan, Dr. Peter Friess, River Publishers.

E-Resources:

1. https://nptel.ac.in/courses/106/105/106105166/
2. https://nptel.ac.in/courses/106/105/106105195/
3. https://nptel.ac.in/courses/108/108/108108123/
4. https://nptel.ac.in/courses/108/108/108108098/

Course Outcomes:

After completion of the course, the students will be able to

1. understand the concept of IOT and M2M.
2. analyse IOT architecture and applications in various fields.
3. understand the security and privacy issues in IOT.
4. design Machine to Machine Communication model for different applications.
5. apply IOT in Big Data Analysis.

AY 2022-23 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD I Year – I Sem			
Course Code: LM61I	**HDL SIMULATION LAB**	**L**	**T**	**P**	**D**
Credits: 2		**0**	**0**	**4**	**0**

Course Objectives:

1. To make students familiar with VHDL/Verilog for advanced digital design techniques.
2. To introduce broad coverage of HDL from a practical design perspective.
3. To gain practical knowledge on gate, dataflow (RTL) and behavioral modeling.
4. To demonstrate timing simulation and synthesis for digital circuits.
5. To implement Designed Digital Circuits using FPGA and CPLD devices.

Note: All the following digital circuits are to be designed using XILINX's/ Altera's/ Equivalent CAD tools.

Programming can be done using any HDL compiler, Verification of the Functionality of the module using functional Simulator, Timing Simulator for Critical Path time Calculation, Synthesis of module, Place & Route.

EXPERIMENT 1: Digital Circuits Description using Verilog/ VHDL
EXPERIMENT 2 Verification of the Functionality of designed Circuits using function Simulator.
EXPERIMENT 3: Timing Simulation for critical path time calculation.
EXPERIMENT 4 Synthesis of Digital Circuits.
EXPERIMENT 5: Place and Route techniques for major FPGA vendors such as Xilinx/ Altera/ Actel etc.
EXPERIMENT 6: Implementation of Designed Digital Circuits using FPGA and CPLD devices.

Course outcomes:

At the end of the course, student will be able to

1. understand VHDL/Verilog for advanced digital design techniques.
2. offers broad coverage of HDL from a practical design perspective.
3. demonstrate gate, dataflow (RTL) and behavioral modeling.
4. analyse timing simulation and synthesis for digital circuits.
5. demonstrate Designed Digital Circuits using FPGA and CPLD devices.

AY 2022-23 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD I Year – I Sem			
Course Code: LM61J	**DIGITAL CMOS IC DESIGN LAB**	**L**	**T**	**P**	**D**
Credits: 2		**0**	**0**	**4**	**0**

Course Objectives:

1. To describe over view about evolution of CMOS integrated circuits.
2. To provide knowledge about Combinational, Sequential MOS logic circuits.
3. To introduce and familiarize with the various logic circuits.
4. To prepare them to face the challenges in dynamic logic circuits.
5. To prepare them to design various building blocks in combinational and sequential circuits.

Note: All the following digital circuits are to be designed and implemented using Cadence/ Mentor Graphics/ Synopsys/ equivalent CAD Tools.

EXPERIMENT 1: Design and Draw layout for CMOS Inverter gate and perform DRC, LVS, RC Extraction.

EXPERIMENT 2 Design and Draw layout for CMOS NOR/ NAND gate and perform DRC, LVS, RC Extraction.

EXPERIMENT 3: Design and Draw layout for CMOS XOR gate using Transmission Gates and perform DRC, LVS, RC Extraction.

EXPERIMENT 4 Design and Draw layout for Full Adder using CMOS logic and perform DRC, LVS, RC Extraction.

EXPERIMENT 5: Design and Draw layout for Latch using CMOS logic and perform DRC, LVS, RC Extraction.

EXPERIMENT 6: Design and Draw layout for SRAM Design using CMOS logic and perform DRC, LVS, RC Extraction.

Course Outcomes:

After completion of the course, the students will be able to

1. know about the various Combinational and Sequential MOS logic circuits.
2. gain in-depth knowledge of applying the concepts on real time applications.
3. understand the basic concepts of Boolean expressions.
4. design different Combinational logic blocks.
5. analyze and implement various memory elements.

AY 2022-23 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech VLSISD I Year – I Sem			
Course Code: LM91A	**SOFT SKILLS (Mandatory Course-I)**	**L**	**T**	**P**	**D**
Credits: 2		**2**	**0**	**0**	**0**

Pre-requisite: Nil

Course Objectives:

This course will enable students to

1. study the Positivity, Motivation and developing positive thinking and attitude.
2. summarize the listening skills and essential formal writing skills.
3. explain the Time Management and Personality Development.
4. describe the Decision-Making and Problem-Solving Skills.
5. study the Psychometric Analysis and Mock Interview Sessions.

Module 1

Unit-1: Soft Skills

Soft Skills: An Introduction – Definition and Significance of Soft Skills; Process, Importance and Measurement of Soft Skill Development. Self-Discovery: Discovering the Self; Setting Goals; Beliefs, Values, Attitude, Virtue.

Unit-2: Positivity and Motivation

Positivity and Motivation: Developing Positive Thinking and Attitude; Driving out Negativity; Meaning and Theories of Motivation; Enhancing Motivation Levels.

Module 2

Unit-1: Interpersonal Communication

Interpersonal Communication: Interpersonal relations; communication models, process, and barriers; team communication; developing interpersonal relationships through effective communication; listening skills; essential formal writing skills.

Unit-2: Corporate Communication Styles

Corporate communication styles – assertion, persuasion, negotiation. Public Speaking: Skills, Methods, Strategies and Essential tips for effective public speaking. Group Discussion: Importance, Planning, Elements, Skills assessed; Effectively disagreeing, Initiating, Summarizing and Attaining the Objective. Non-Verbal Communication: Importance and Elements; Body Language. Teamwork and Leadership Skills: Concept of Teams; Building effective teams; Concept of Leadership and honing Leadership skills.

Module 3

Unit-1: Interview Skills

Interview Skills: Interviewer and Interviewee – in-depth perspectives. Before, During and After the Interview. Tips for Success. Presentation Skills: Types, Content, Audience Analysis, Essential Tips – Before, During and After, Overcoming Nervousness. Etiquette and Manners – Social and Business.

Unit-2: Time Management

Time Management – Concept, Essentials, Tips. Personality Development – Meaning, Nature, Features, Stages, Models; Learning Skills; Adaptability Skills.

Module 4

Unit-1: Decision-Making and Problem-Solving Skills

Decision-Making and Problem-Solving Skills: Meaning, Types and Models, Group and Ethical Decision-Making, Problems and Dilemmas in application of these skills. Conflict Management: Conflict - Definition, Nature, Types and Causes; Methods of Conflict Resolution.

Unit-2: Stress Management

Stress Management: Stress - Definition, Nature, Types, Symptoms and Causes; Stress Analysis Models and 8 Impact of Stress; Measurement and Management of Stress, Leadership and Assertiveness Skills: A Good Leader; Leaders and Managers; Leadership Theories; Types of Leaders; Leadership Behaviour; Assertiveness Skills. Emotional Intelligence: Meaning, History, Features, Components, Intrapersonal and Management Excellence; Strategies to enhance Emotional Intelligence.

Module 5

Unit-1: Employability Skills

Employability Skills: Resume buildings – Facing the Personal Interview (HR and Technical)- Psychometric Analysis-Mock Interview Sessions.

Text Books/ Reference Books:

1. Managing Soft Skills for Personality Development –edited by B.N.Ghosh, McGraw Hill India, 2012.
2. English and Soft Skills – S.P.Dhanavel, Orient BlackswanIndia, 2010.

E-Resources:

1. http://nptel.ac.in/downloads

Course outcomes:

After completion of the course, the students will be able to

1. describe the Positivity, Motivation and developing positive thinking and attitude.
2. explain the listening skills and essential formal writing skills.
3. discuss the Time Management and Personality Development.
4. illustrate the Decision-Making and Problem-Solving Skills.
5. describe the Psychometric Analysis and Mock Interview Sessions.

AY 2022-23 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech VLSISD I Year – II Sem			
Course Code: LM62A	**ANALOG CMOS IC DESIGN**	**L**	**T**	**P**	**D**
Credits: 3		**3**	**0**	**0**	**0**

Pre-requisite: Basics of VLSI and CMOS.

Course Objectives:

1. To describe over view about evolution of CMOS integrated circuits.
2. To provide knowledge about fabrication process and technology.
3. To provide knowledge about Analog CMOS Sub-Circuits and current mirrors.
4. To introduce and familiarize with the various Amplifiers & OP-amps.
5. To prepare them to face the challenges in CMOS technology.

Module 1
Unit 1: MOS Devices and Modeling
The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters.
Unit 2: Small-Signal Model for the MOS Transistor
Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

Module 2
Unit 1: Analog CMOS Sub-Circuits
MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources.
Unit 2: Current Mirrors
Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode Current mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

Module 3
Unit 1: CMOS Amplifiers
Inverters, Differential Amplifiers, Cascode Amplifiers.
Unit 2: Current Amplifiers
Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

Module 4
Unit 1: CMOS Operational Amplifiers
Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power-Supply Rejection Ratio of Two-Stage Op Amps.
Unit 2 : Cascode Op Amps
Cascode Op Amps, Measurement Techniques of OP Amp.

Module 5
Unit 1: Comparators
Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop, Comparators.
Unit 2 : Improving the Performance of Open-Loop Comparators
Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

Text Books:

1. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
2. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.

Reference Books:

1. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edn, 2013.
2. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition.
3. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.

E-Resources:

1. https://nptel.ac.in/courses/117/101/117101105/
2. https://nptel.ac.in/courses/117/106/117106093/
3. https://nptel.ac.in/courses/108/107/108107129/

Course Outcomes:

After completion of the course, the students will be able to

1. develop an in-depth understanding of the design principles and applications of CMOS Analog IC design.
2. know the fabrication steps involved in CMOS technology.
3. become familiar with the small signal and large signal models of CMOS transistors.
4. gain knowledge of applying the concepts on real time applications.
5. analyze and design of CMOS op Amps and compensation techniques.

AY 2022-23 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD I Year – II Sem			
Course Code: LM62B	LOW POWER VLSI DESIGN	L	T	P	D
Credits: 3		3	0	0	0

Pre-requisite: VLSI, Electronics Devices and Circuits, Digital Electronics.

Course Objectives:

1. This course addresses a profound analysis on the development of the CMOS & Bi-CMOS digital circuits for a low voltage low power environment.
2. To study the concepts of device behavior and modeling.
3. To study the concepts of low voltage, low power logic circuits.
4. To understand the concepts of low power memory design.
5. To understand the basics of low power Microprocessor design.

Module 1

Unit-1: Technology & Circuit Design Levels

Sources of power dissipation in digital ICs, degree of freedom, recurring themes in low-power, emerging low power approaches, dynamic dissipation in CMOS, effects of Vdd & Vt on speed, constraints on Vt reduction, transistor sizing & optimal gate oxide thickness, impact of technology scaling, technology innovations.

Module 2

Unit-1: Low Power Circuit Techniques

Power consumption in circuits, flip-flops & latches, high capacitance nodes, energy recovery, reversible pipelines, high performance approaches.

Unit-2: Low Power Clock Distribution

Low Power Clock Distribution: Power dissipation in clock distribution, single driver.

Module 3

Unit-1: Logic Synthesis for Low Power estimation techniques

Power minimization techniques, low power arithmetic components- circuit design styles, adders, multipliers.

Module 4

Unit-1: Low Power Memory Design

Sources & reduction of power dissipation in memory subsystem, sources of power dissipation in DRAM & SRAM, low power DRAM circuits, low power SRAM circuits.

Module 5

Unit-1: Low Power Microprocessor Design System

Power management support, architectural tradeoffs for power, choosing the supply voltage, low-power clocking, implementation problem for low power, comparison of microprocessors for power & performance.

Text Books:

1. P. Rashinkar, Paterson and L. Singh, "Low Power Design Methodologies", Kluwer Academic, 2002.
2. Kaushik Roy, Sharat Prasad, "Low power CMOS VLSI circuit design", John Wiley sons Inc.,2000.

References Books:

1. J.B.Kulo and J.H Lou, "Low voltage CMOS VLSI Circuits", Wiley, 1999.
2. A.P.Chandrasekaran and R.W.Broadersen, "Low power digital CMOS design", Kluwer,1995.
3. Gary Yeap, "Practical low power digital VLSI design", Kluwer, 1998.

E - Resources:

1. http://nptel.ac.in/downloads

Course Outcomes:

After completion of the course, the Student will be able to

1. identify the sources of power dissipation in digital IC systems.
2. understand the impact of power on system performance and reliability.
3. characterize and model power consumption & understand the basic analysis methods.
4. understand leakage sources and reduction techniques.
5. illustrate the basics of low power Microprocessor design.

AY 2022-23 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD I Year – II Sem			
Course Code: LM62C	VLSI SIGNAL PROCESSING (Program Elective –III)	L	T	P	D
Credits: 3		3	0	0	0

Pre-requisite: VLSI Technology and Digital Signal Processing

Course Objectives:

1. To describe the types of DSP algorithms and pipeline methodology.
2. To provide knowledge about Folding and Unfolding Techniques.
3. To provide knowledge about Systolic Architecture Design and Fast Convolution.
4. To describe Fast Convolution and iterated convolution techniques.
5. To illustrate Low Power Design and Programmable DSP.

Module 1

Unit-1: Introduction to DSP

Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms.

Unit –2: Pipelining and Parallel Processing

Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power.

Retiming: Introduction, Definitions and Properties, Solving System of Inequalities, Retiming Techniques.

Module 2

Unit –1: Folding

Introduction, Folding Transform, Register minimization techniques, Register minimization in folded architectures, folding of Multirate systems.

Unit –2: Unfolding

Introduction, An Algorithm for Unfolding, Properties of Unfolding, Critical Path, Unfolding and Retiming, Applications of Unfolding.

Module 3

Unit -1: Systolic Architecture Design

Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector.

Unit -2: Matrix Multiplication

Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations contain Delays.

Module 4

Unit-1: Fast Convolution

Introduction – Cook-Toom Algorithm – Winogard algorithm.

Unit-2: Iterated Convolution

Cyclic Convolution – Design of Fast Convolution algorithm by Inspection.

Module 5

Unit-1: Low Power Design

Scaling Vs Power Consumption, Power Analysis, Power Reduction Techniques, Power Estimation Approaches.

Unit-2: Programmable DSP

Evaluation of Programmable Digital Signal Processors, DSP Processors for Mobile and Wireless Communications, Processors for Multimedia Signal Processing.

Text Books

1. VLSI Digital Signal Processing- System Design and Implementation – Keshab K. Parthi, Wiley Inter Science, 1998.
2. VLSI and Modern Signal processing – Kung S. Y, H. J. While House, T. Kailath, Prentice Hall, 1985.

References

1. Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing – Jose E. France, Yannis Tsividis, Prentice Hall, 1994.
2. VLSI Digital Signal Processing – Medisetti V. K, IEEE Press (NY), 1995.

E-Resources:

1. https://nptel.ac.in/courses/108/105/108105157/
2. https://onlinecourses.nptel.ac.in/noc20_ee44/

Course Outcomes:

After completion of the Course, students will be able to

1. modify the existing or new DSP architectures suitable for VLSI.
2. describe the concepts of folding and unfolding algorithms and applications.
3. implement fast convolution algorithms.
4. understand low power design aspects of processors for signal processing and wireless applications.
5. illustrate the concepts of Systolic Architecture Design and Matrix Multiplication.

AY 2022-23 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD I Year – II Sem			
Course Code: LM62D	RF IC ARCHITECTURE (Program Elective -III)	L	T	P	D
Credits: 3		3	0	0	0

Pre-requisite: Wireless Communication and Electronic Devices and Circuits.

Course Objectives:

1. To learn the basic elements of Analog and digital systems design.
2. To understand the Random process, noise, sensitivity and dynamic range.
3. To learn about the various FDMA, TDMA, CDMA, Wireless standards.
4. To understand the Oscillators, Frequency synthesizers performance.
5. To enrich the knowledge about High Frequency power amplifier**.**

Module 1

Unit-1: Introduction to RF and Wireless Technology

Complexity comparison, Design bottle necks, Applications, Analog and digital systems, Choice of Technology.

Module 2

Unit-1: Basic concepts in RF Design

Nonlinearity and time variance, ISI, Random process and noise, sensitivity and dynamic range, passive impedance transformation.

Module 3

Unit-1: Multiple Access

Techniques and wireless standards, mobile RF communication, FDMA, TDMA, CDMA, Wireless standards.

Unit-2: Transceiver Architectures

General considerations, Receiver architecture, Transmitter Architecture, Transceiver performance tests, case studies.

Module 4

Unit-1: Amplifiers, Mixers and Oscillators

LNAs, down conversion mixers, Cascaded Stages, oscillators, Frequency synthesizers.

Module 5

Unit-1: Power Amplifiers

General considerations, linear and nonlinear Pas, classification, High Frequency power amplifier, large signal impedance matching, linearization techniques.

Text Books:

1. Behzad Razavi, RF Microelectronics Prentice Hall of India, 2001.
2. Thomas H. Lee, The Design of CMOS Radio Integrated Circuits**,** Cambridge University Press.

Reference Books:

1. T.H.Lee,"The Design of CMOS Radio-Frequency Integrated Circuits", Cambridge University Press, 2nd, 1998.
2. R.Jacob Baker, Harry W.Li, D.E. Boyce, "CMOS Circuit Design, Layout and Simulation", Prentice-Hall of India, 1998.

E-Resources:

1. **https://youtu.be/KUDGGsyh1Hs**
2. **https://youtu.be/cHbcdk-C4Zo**

Course Outcomes:

After completion of the course, the students will be able to

1. demonstrate in-depth knowledge in limitations of Low Power Design, SOI Technology.
2. analyze the Random process, sensitivity and dynamic range for conducting research in ULSI design.
3. solve problems of FDMA, TDMA, CDMA, Wireless standards.
4. analyze the oscillators, Frequency synthesizer's performance.
5. apply appropriate techniques, resources and tools to engineering activities in High Frequency power amplifier.

AY 2022-23 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD I Year – II Sem			
Course Code: LM62E	SOC DESIGN (Program Elective-III)	L	T	P	D
Credits: 3		3	0	0	0

Pre-requisite: VLSI Technology

Course Objectives:

1. To understand CISC, RISC and NISC approaches for SOC.
2. To understand NISC architectures and embedded processors.
3. To understand reconfigurable systems.
4. To design and optimise Low power system.
5. To understand the Concept of graph theory and learn different approaches for synthesis.

Module 1

Unit-1: **ASIC**

Overview of ASIC types, design strategies, CISC, RISC and NISC approaches for SOC.

Unit-2: Architectural Issues

Architectural issues and its impact on SOC design methodologies, Application Specific Instruction, Processor (ASIP) concepts.

Module 2

Unit -1: **NISC**

NISC Control Words methodology, NISC Applications and Advantages, Architecture Description Languages (ADL) for design and verification of Application Specific Instruction Set.

Unit-2: **Processors**

ASIP, No-Instruction-Set-computer (NISC)- design flow, Modeling NISC architectures and systems, use of Generic Netlist Representation - A formal language for specification, compilation and synthesis of embedded processors.

Module 3

Unit-1: **Simulation**

Different simulation modes, behavioural, functional, static timing, gate level, switch level, transistor/circuit simulation, design of verification vectors, Low power FPGA, Reconfigurable systems, SOC related Modeling of data path design and control logic, Minimization of interconnects impact, clock tree design issues.

Module 4

Unit-1: Low power SOC design / Digital system

Design synergy, Low power system perspective- power gating, clock gating, Adaptive Voltage Scaling (AVS), Static Voltage Scaling, Dynamic Clock Frequency and Voltage Scaling (DCFS), building block optimization, building block memory, power down techniques, power consumption verification.

Module 5

Unit-1: **Synthesis**

Role and Concept of graph theory and its relevance to synthesizable constructs, Walks, trails paths, connectivity, components, mapping/visualization, nodal and admittance graph.

Unit-2: **Approaches**

Technology independent and technology dependent approaches for synthesis, optimization constraints, Synthesis report analysis, Single core and Multi core systems, dark silicon issues, HDL coding techniques for minimization of power consumption, Fault tolerant designs.

Text Books:

1. Hubert Kaeslin, "Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication", Cambridge University Press, 2008.

2. B. Al Hashimi, "System on chip-Next generation electronics", The IET, 2006.

Reference Books:

1. Rochit Rajsuman, "System-on- a-chip: Design and test", Advantest America R & D Center, 2000.

2. P Mishra and N Dutt, "Processor Description Languages", Morgan Kaufmann, 2008.

3. Michael J. Flynn and Wayne Luk, "Computer System Design: System-on-Chip". Wiley, 2011.

E-Resources:

1. http://nptel.ac.in/downloads

Course Outcomes:

At the end of the course, student will be able to:

1. understand CISC, RISC and NISC approaches for SOC

2 understand NISC architectures and embedded processors.

3. understand reconfigurable systems

4 design and optimise Low power system.

5. understand the Concept of graph theory and learn different approaches for synthesis

AY 2022-23 Onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD I Year – II Sem			
Course Code: LM62F	**HARDWARE SOFTWARE CO-DESIGN (Program Elective -IV)**	**L**	**T**	**P**	**D**
Credits: 3		**3**	**0**	**0**	**0**

Pre-requisite: Embedded Systems

Course Objectives:
This course will enable students to

1. describe an embedded system design flow from specification to physical realization.
2. describe structural behavior of systems.
3. master complex systems.
4. devise new theories, techniques and tools in design, implementation and testing.
5. master contemporary development techniques.

Module 1
Unit-1: Co- Design Issues
Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.
Unit-2: Co- Synthesis Algorithms
Hardware software synthesis algorithms: hardware – software partitioning, distributed system co-synthesis.

Module 2
Unit-1: Prototyping and Emulation
Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure.
Unit-2: Target Architectures
Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

Module 3
Unit-1: Compilation Techniques and Tools for Embedded Processor Architectures
Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

Module 4
Unit-1: Design Specification and Verification
Design, co-design, the co-design computational model, concurrency coordinating concurrent Computations, interfacing components design verification, implementation verification, verification tools, interface verification.

Module 5
Unit-1: Languages for System – Level Specification and Design-I
System – level specification, design representation for system level synthesis, system level Specification languages.
Unit-2: Languages for System – Level Specification and Design-II
Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos System.

Text Books:
1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf –2009, Springer.
2. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, 2002, Kluwer Academic Publishers.

Reference Books:
1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont – springer.

E - Resources:
1. https://www.cs.ccu.edu.tw/~pahsiung/courses/soc/notes/SoC_Design_Flow_Tools_Codesign.pdf
2. https://www.sciencedirect.com/book/9781558607026/readings-in-hardware- software-co-design
3. https://nptel.ac.in/content/storage2/courses/108105057/Pdf/Lesson-1.pdf

Course Outcomes:

After completion of the course, the student will be able to

1. gain knowledge of contemporary issues and algorithms used.
2. Know the interfacing components, different verification techniques and tools.
3. demonstrate practical skills in the construction of prototypes.
4. understand the use of modern hardware and software tools for building prototypes of embedded systems.
5. apply embedded software techniques to satisfy functional and response time requirements.

AY 2022-23 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD I Year – II Sem			
Course Code: LM62G	IMAGE AND VIDEO PROCESSING (Program Elective -IV)	L	T	P	D
Credits: 3		3	0	0	0

Pre-requisite: Vector Algebra, DSP, Filtering Methods.

Course Objectives:

1. To understand representation of digital images and video in the spatial (pixel) and frequency domains and learn common digital video formats.
2. To understand spatial and temporal resolution and aliasing; understand basic image and video filtering operations.
3. To understand principles and methods of motion/optical flow estimation; understand fundamentals of image compression.
4. To study fundamentals of video compression.
5. To learn recent image and video compression standards.

Module 1

Unit 1: Fundamentals of Image Processing

Basic steps of Image Processing System, Sampling and Quantization of an image, Basic relationship between pixels.

Unit 2: Image Segmentation

Segmentation concepts, Point, Line and Edge Detection, Thresholding, Region based segmentation.

Module 2

Unit 1: Spatial domain methods

Histogram processing, Fundamentals of Spatial filtering, Smoothing spatial filters, Sharpening spatial filters.

Unit 2: Frequency domain methods

Basics of filtering in frequency domain, Image smoothing, Image sharpening, Selective filtering.

Module 3

Unit 1: Image compression fundamentals

Coding Redundancy, Spatial and Temporal redundancy.

Unit 2: Compression models

Lossy & Lossless Huffman coding, Bit plane coding, Transform coding, Predictive coding, Wavelet coding, Lossy Predictive coding, JPEG Standards.

Module 4

Unit 1: Basic Steps of Video Processing

Analog Video, Digital Video, Time-Varying Image Formation models: Three-Dimensional Motion Models, Geometric Image Formation, Photometric Image Formation.

Unit 2: **Filtering Methods**

Sampling of Video Signals, Filtering operations.

Module 5

Unit 1: 2-D Motion Estimation

Optical flow, General Methodologies, Pixel Based Motion Estimation, Block-Matching Algorithm, Mesh based Motion Estimation, Global Motion Estimation, Region based Motion Estimation, Multi resolution motion estimation.

Unit 2: Coding Method

Waveform based coding, Block based transform coding, Predictive coding, Application of motion estimation in video coding.

Text Books:

1. Digital Image Processing – Gonzalez and Woods, 3rd Ed., Pearson.
2. Video Processing and Communication – Yao Wang, Joem Ostermann and Ya quin Zhang. 1st Ed., PH Int.

Reference Books:

1. Digital Image Processing using MATLAB– Gonzalez and Woods, 2nd ed., Mc Graw Hill Education, 2010.
2. Image Processing Analysis, and Machine Vision- Milan Sonka, Vaclan Hlavac, 3 ed., CENGAGE, 2008.
3. Digital Video Processing – A Murat Tekalp, PERSON, 2010.
4. Digital Image Processing – S.Jayaraman, S.Esakkirajan, T.Veera Kumar –TMH, 2009.

E- Resources:

1.https://nptel.ac.in/courses/117/105/117105079/

2. https://www.coursera.org/learn/digital

3.https://ocw.mit.edu/resources/res-2-006-girls-who-build-cameras-summer-2016/image-processing/

Course Outcomes:

After completion of the course, the student will be able to

1. understand image processing concepts of Thresholding and Segmentation.
2. analyse various spatial and frequency domain filtering techniques.
3. implement various image and video compression methods and standards.
4. Explore different video processing models and filtering techniques.
5. able to build motion models and video coding procedures and apply them for motion estimation.

AY 2022-23 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD I Year – II Sem			
Course Code: LM62H	DESIGN FOR TESTABILITY (Program Elective -IV)	L	T	P	D
Credits: 3		3	0	0	0

Pre-requisite: VLSI Technology

Course Objectives:

1. To provide knowledge about VLSI Testing.
2. To understand VLSI Technology trends affecting Testing.
3. To get knowledge on Design Verification and Test Evaluation.
4. To understand the concept of BIST architecture.
5. To provide knowledge about Boundary Scan Test.

Module 1

Unit 1: Introduction to Testing

Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology trends affecting Testing, Types of Testing.

Unit 2: Fault Modeling

Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

Module 2

Unit 1: Logic and Fault Simulation

Simulation for Design Verification and Test Evaluation, Algorithms for Fault Simulation, ATPG.

Unit 2: True Value Simulation

Modeling Circuits for Simulation Algorithms for True-Value Simulation.

Module 3

Unit 1: Testability Measures

SCOAP Controllability and Observability, High Level Testability Measures.

Unit 2: DFT Methods and Scan Design

Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

Module 4

Unit 1: Built-In Self-Test

The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers.

Unit 2: BIST Systems Scans

Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST

Module 5

Unit 1: Boundary Scan Standard

Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard.

Unit 2: Boundary Scan Description Language

BDSL Description Components, Pin Descriptions.

Text Books:

1. Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits - M.L. Bushnell, V. D. Agrawal, Kluwer Academic Publishers.

eference Books:

1. Digital Systems and Testable Design - M. Abramovici, M.A.Breuer and A.D Friedman, Jaico Publishing House.
2. Digital Circuits Testing and Testability - P.K. Lala, Academic Press.

E-Resources:

1. https://onlinecourses.nptel.ac.in/noc20_ee76/
2. https://nptel.ac.in/courses/106/103/106103116/

Course Outcomes:

After completion of the course, the student will be able to

1. create understanding of the fundamental concepts of Testing in VLSI design.
2. perceiving trends affecting Testing
3. understand the high level testability measures and scan methods.
4. illustrate the BIST architecture: Test pattern generation, Circuit under test and Output response analyzer.
5. develop skills in modeling and evaluating Boundary Scan Standards.

AY 2022-23 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD I Year – II Sem			
Course Code: LM92A	**RESEARCH METHODOLOGY AND IPR (Common to M.Tech - EPS, VLSISD, CAD-CAM, CSE & SE)**	**L**	**T**	**P**	**D**
Credits: 2		**2**	**0**	**0**	**0**

Pre-requisiste: Nil

Course Objectives:

1. To understand the basic concept of research problem formulation.
2. To be exposed to effective research report writing and research design.
3. To investigate the various methods of data collection and analysis.
4. To understand the various fields of Industrial Property and PCT.
5. To be exposed to administration of IP and new developments in IPR.

Module 1

Unit 1: Introduction

Meaning and Objectives of Research, Types of Research, Research Approaches, Research Methods Vs Methodology, Research Process, Criteria of Good Research.

Unit 2: Research Problem

Meaning of Research Problem, Steps involved in Selecting a Research Problem, Scope and Objectives of Research Problem, Sources of Research Problem, Characteristics of a Good Research Problem, Steps involved in Defining a Research Problem.

Module 2

Unit 1: Effective technical writing

Importance of Literature Review, Steps involved in conducting a Literature Review, Research Report, Characteristics of a Good Report, Layout of a Research Report, Writing a Journal Paper, Writing a Research Proposal, Format of Research Proposal, Plagiarism and Research Ethics.

Unit 2: Research Design

Need for Research Design, Features of a Good Design, Important Concept Relating to Research Design, Categories of Research Design.

Module 3

Unit 1: Data Collection

Methods of Primary Data Collection – Observation Method, Interview Method, Collection of Data through Questionnaire and Schedule, Collection of Secondary Data, Selection of Appropriate Method for Data Collection.

Unit 2: Data Processing and Analysis

Processing Operations, Problems in Processing, Types of Analysis, Multivariate Analysis, Correlation Analysis, Regression Analysis.

Module 4

Unit 1: Fields of Intellectual Protection

Patents - Conditions of Patentability, Drafting and Filing a Patent Application, Examination of a Patent Application; Copyright - Copyright Protection, Subject Matter of Copyright Protection, Ownership of Copyright, Limitations on Copyright Protection; Trademarks - Definitions, Criteria of Protectability, Protection of Trademark Rights; Industrial Designs; Geographical Indications.

Unit 2: International cooperation on intellectual property

World Intellectual Property Organization (WIPO) - Patenting under PCT; Patent information and databases; Licensing and transfer of technology.

Module 5

Unit 1: Administration of Industrial Property

Administrative Structure in the Industrial Property Office, Patent Office, Trademark Office, Industrial Designs Office, Patent and Trademark Attorney.

Unit 2: New Developments in IPR

Technological and Legal Developments in Intellectual Property, Traditional Knowledge, Case Studies.

Text Books:

1.Stuart Melville and Wayne Goddard, "Research Methodology: An Introduction for Science & Engineering Students'', Juta & Co. Ltd Publishers, Revised Second Edition, 2006.
2.Halbert, "Resisting Intellectual Property", Routledge, Taylor & Francis Ltd, First Edition, 2007.
3.C. R. Kothari, "Research Methodology: Methods and Techniques", New Age International Publications, Revised Second Edition, 2004.

Reference Books:

1. Ranjit Kumar, "Research Methodology: A Step by Step Guide for beginners", British Library Publishers, Fourth Edition, 2014.
2. Robert P. Merges, Peter S. Menell, Mark A. Lemley, "Intellectual Property in New Technological Age", Wolters Kluwer Law & Business Publishers, 2016.
3. T. Ramappa, "Intellectual Property Rights Under WTO", S. Chand Publications, First Edition, 2008.

E-Resources:

1. http://nptel.ac.in/downloads

Course Outcomes:

At the end of this course, students will be able to

1.Understand the basic concept of research problem formulation.
2.Develop an effective research proposal and research report.
3.Identify appropriate method for data collection and analysis for effective research.
4.Apply for Patent Filing and other fields of IP.

AY 2022-23 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD I Year – II Sem			
Course Code: LM62I	ANALOG CMOS IC DESIGN LAB	L	T	P	D
Credits: 2		0	0	4	0

Course Objectives:

1. To describe over view about evolution of CMOS integrated circuits.
2. To provide knowledge about fabrication process and technology.
3. To introduce and familiarize with the various Amplifiers & OP-amps.
4. To prepare them to face the challenges in CMOS technology.
5. To perform DRC, LVS and RC Extraction.

Note: All the following digital circuits are to be designed and implemented using Cadence/ Mentor Graphics/ Synopsys/ equivalent CAD Tools.

1. **EXPERIMENT 1**: Analyze the NMOS and PMOS Operating point Characteristics.
2. **EXPERIMENT 2** Design a CMOS Current Mirror and find out the AC, DC, OP analysis.
3. **EXPERIMENT 3**: Design a NMOS Differential Amplifier and find out the AC, DC, OP analysis.
4. **EXPERIMENT 4** Design a PMOS Differential Amplifier and find out the AC, DC, OP analysis.
5. **EXPERIMENT 5**: Design a CMOS Operational Amplifier and find out the AC analysis and noise margin analysis.
6. **EXPERIMENT 6:** Design a comparator using Operational Amplifier and find out the AC analysis.
7. **EXPERIMENT 7:** Draw the Analog Layout for CMOS current Mirror and perform DRC, LVS, RC Extraction.

Course Outcomes:

After completion of the course, the student will be able to

1. develop an in-depth understanding of the design principles and applications of CMOS Analog IC design.
2. to know the fabrication steps involved in CMOS technology.
3. be familiar with the small signal and large signal models of CMOS transistors.
4. have an in-depth knowledge of applying the concepts on real time applications.
5. analyze and design of CMOS Op Amps and compensation techniques.

AY 2022-23 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD I Year – II Sem			
Course Code: LM62J	**VLSI DESIGN AND VERIFICATION LAB**	**L**	**T**	**P**	**D**
Credits: 2		**0**	**0**	**4**	**0**

Course Objectives:

1. To familiarize basic principles of VLSI Circuit design and layout design.
2. To familiarize the performance verification metrics of digital circuits such as FIFO, Finite State machines, UART module with FIFO interface.
3. To introduce synthesis method to different designs.
4. To design serial port and integration within a system.
5. To implement digital designs in physical layout.

Note: All the following digital circuits are to be designed and implemented using Xilinx/Cadence/ Mentor Graphics/ Synopsys/ equivalent CAD Tools.

1. Connect two of such FIFOs having different clock rates. Design and test a 2 location 4-bit wide FIFO. Explain the problems associated with such a setup.

2. Building and testing a parameterised multi-bit adder using control swap (Fredkin) gates as building blocks.

3. Example of some basic circuits, finite state machines (Moore/Mealy).
    a. Test and debug code for muxes, encoder/decoders, counters, memory access.

4. Serial port design and integration within a system.
    a. Test and debug the code for a UART module with a FIFO interface. Connect two UART modules and transmit/receive data between them.

5. Introduction to synthesis. (Implement any one)
    a) Run a program to blink an LED on the FPGA.
    b) Establish a serial communication between board and computer host.
    c) Establish wired/wireless communication between FPGA to FPGA.

6. Any of the above designs, implement the physical layout.

Course Outcomes:

On completion of the course, student will be able to

1. understand the necessity of VLSI system design and verification.
2. apply the constraints posed by the VLSI fabrication technology to design and verify digital circuits.
3. apply the backend tools efficiently and apply to build digital circuits.
4. apply synthesis to various real time programs.
5. implement the physical layout design for digital circuits.

AY 2022-23 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech VLSISD I Year – II Sem			
Course Code: LM92B	**PERSONALITY DEVELOPMENT AND PROFESSIONAL VALUES (Mandatory Course-II)**	**L**	**T**	**P**	**D**
Credits: 2		**2**	**0**	**0**	**0**

Pre-requisite: Nil

Course Objectives:

This course will enable students to

1. Study the sensitization towards gender equality, physically challenged, intellectually challenged.
2. Summarize the Leadership and qualities of a successful leader.
3. Explain the Modern Challenges of Adolescent Emotions and behaviour.
4. Describe the Personality Development Body language.
5. Study the Workplace Rights & Responsibilities.

Module 1

Unit 1: Concept of Human Values, Value Education Towards Personal Development

Aim of education and value education; Evolution of value-oriented education; Concept of Human values; types of values; Components of value education.

Unit 2: Personal Development

Personal Development: Self-analysis and introspection; sensitization towards gender equality, equitability, physically challenged, intellectually challenged. Respect to - age, experience, maturity, family members, neighbours, co-workers.

Unit 3: Character Formation Towards Positive Personality

Character Formation Towards Positive Personality: Truthfulness, Constructively, Sacrifice, Sincerity, Self-Control, Altruism, Tolerance, Scientific Vision.

Module 2

Unit 1: Aspects of Personality Development

Aspects of Personality Development **-**Body language- Problem-solving - Conflict and Stress Management - Decision-making skills - Leadership and qualities of a successful leader – Character building -Team-works - Positive attitude – Advantages –Negative attitude- Disadvantages– Time management - Work ethics –Good manners and etiquette.

Module 3

Unit 1: Professional Practices in Engineering

Professional Practices in Engineering: Professions and Norms of Professional Conduct, Norms of Professional Conduct vs. Profession; Responsibilities, Obligations and Moral Values in Professional Ethics, Professional codes of ethics, the limits of predictability and responsibilities of the engineering profession.

Unit 2: Central Responsibilities of Engineers

Central Responsibilities of Engineers - The Centrality of Responsibilities of Professional Ethics; lessons from 1979 American Airlines DC-10 Crash and Kansas City Hyatt Regency Walk away Collapse.

Module 4

Unit 1: Workplace Rights & Responsibilities

Workplace Rights & Responsibilities, Ethics in changing domains of Research, Engineers and Managers; Organizational Complaint Procedure, difference of Professional Judgment within the Nuclear Regulatory Commission (NRC), the Hanford Nuclear Reservation.

Module 5

Unit 1: Impact of Global Development on Ethics and Values

Impact of Global Development on Ethics and Values: Conflict of cross-cultural influences, mass media, cross-border education, materialistic values, professional challenges, and compromise. Defining the difference between aggressive, submissive, and assertive behaviours, Modern Challenges of Adolescent Emotions and behaviour.

Unit 2: Sex and spirituality

Sex and spirituality: Comparison and competition; positive and negative thoughts. Adolescent Emotions, arrogance, anger, sexual instability, selfishness, defiance.

Text Books:

1. Hurlock, E.B (2006). Personality Development, 28th Reprint. New Delhi: Tata McGraw Hill.
2. Stephen P. Robbins and Timothy A. Judge(2014), Organizational Behavior 16th Edition: Prentice Hall.

Reference Books:

1. Andrews, Sudhir. How to Succeed at Interviews. 21st (rep.) New Delhi, Tata McGraw-Hill 1988.
2. Heller, Robert. Effective leadership. Essential Manager series. Dk Publishing, 2002.
3. Hindle, Tim. Reducing Stress. Essential Manager series. Dk Publishing, 2003.
4. Lucas, Stephen. Art of Public Speaking. New Delhi. Tata - Mc-Graw Hill. 2001.

E-Resources:

1. http://nptel.ac.in/downloads

Course Outcomes:

On completion of the course, the students will be able to

1. describe the sensitization towards gender equality, physically challenged, intellectually challenged.
2. explain the Leadership and qualities of a successful leader.
3. discuss the Modern Challenges of Adolescent Emotions and behaviour.
4. illustrate the Personality Development Body language.
5. identify the Workplace Rights & Responsibilities.

AY 2022-23 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD II Year – I Sem			
Course Code: LM63A	**MEMORY TECHNOLOGIES (Program Elective -V)**	**L**	**T**	**P**	**D**
Credits: 3		**3**	**0**	**0**	**0**

Pre-requisite: Computer Organization and Architecture.

Course Objectives:

The Students will

1. select architecture and design semiconductor memory circuits and subsystems.
2. explore various fault models, modes and mechanisms in semiconductor memories.
3. gain knowledge on various advanced memory technologies.
4. identify memory testing and reliability issues.
5. describe the state-of-the-art memory chip design.

Module 1

Unit-1: Random Access Memory Technologies

Static Random Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM.

Unit-2: Advanced SRAM Architectures

Advanced SRAM Architectures, Application Specific SRAMs.

Module 2

Unit-1: DRAMs

DRAMs, MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM.

Unit-2: Advanced DRAM

Advanced DRAM Design and Architecture, Application Specific DRAMs, SRAM and DRAM Memory controllers.

Module 3

Unit-1: Non-Volatile Memories

Masked ROMs, PROMs, Bipolar & CMOS PROM.

Unit-2: EEPROMs

EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Non-volatile SRAM, Flash Memories.

Module 4

Unit-1: Advanced Memory technologies

Advanced Memory Technologies and High-density Memory Packing Technologies, Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random Access Memories (MRAMs), Experimental Memory Devices.

Module 5

Unit-1: Memory Hybrids and Stacks

Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues, Memory Cards, High Density Memory Packaging.

Text Books:

1. Ashok K Sharma, "Advanced Semiconductor Memories: Architectures, Designs and Applications", Wiley Interscience.
2. Kiyoo Itoh, "VLSI memory chip design", Springer International Edition.

Reference Books:

1. Ashok K Sharma," Semiconductor Memories: Technology, Testing and Reliability, PHI.

E - Resources:

1. https://www.youtube.com/watch?v=5CL8iFrbCUg
2. https://www.youtube.com/watch?v=as1lc9u96jI
3. https://freevideolectures.com/course/3523/computer-architecture-i/28

Course Outcomes:

On completion of the course, the students will be able to

1. select architecture and design semiconductor memory circuits and subsystems.
2. identify various fault models, modes and mechanisms in semiconductor memories.
3. illustrate principle behind advanced memory technologies.
4. identify memory testing and reliability issues.
5. know the state-of-the-art memory chip design.

AY 2022-23 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD II Year – I Sem			
Course Code: LM63B	CAD FOR VLSI (Program Elective-V)	L	T	P	D
Credits: 3		3	0	0	0

Pre-requisite: Digital Electronics.

Course Objectives:

1. To introduce the fundamentals of Computer-Aided Design tools for the modelling, design, analysis, test and verification of Digital VLSI Systems.
2. To study various physical design methods in VLSI.
3. To understand the concepts behind the VLSI design rules and routing techniques.
4. To use the simulation techniques at various levels in VLSI design flow.
5. To understand the concepts of various algorithms used for floor planning and routing techniques.

Module 1:
Unit 1: VLSI Physical Design Automation
VLSI Design Cycle, New Trends in VLSI Design Cycle, Physical Design Cycle.
Unit 2: New Trends in Physical Design
New Trends in Physical Design Cycle, Design Styles, System Packaging Styles.

Module 2:
Unit 1: Partitioning, Floor Planning
Partitioning – Problem formulation, Classification of Partitioning algorithms, Kernighan-Lin Algorithm, Simulated Annealing.
Floor Planning – Problem formulation, Classification of floor planning algorithms, constraint-based floor planning, Rectangular Dualization.
Unit 2: Pin Assignment and Placement
Pin Assignment – Problem formulation, Classification of pin assignment algorithms, General and channel Pin assignments.
Placement **–** Problem formulation, Classification of placement algorithms, Partitioning based placement algorithms.

Module 3:
Unit 1: Global Routing
Global Routing – Problem formulation, Classification of global routing algorithms, Maze routing algorithms.
Unit 2: Detailed Routing
Detailed Routing – Problem formulation, Classification of routing algorithms, Single layer routing algorithms.

Module 4:
Unit 1: Physical Design Automation of FPGAs
FPGA Technologies, Physical Design cycle for FPGAs, Partitioning, Routing – Routing Algorithm for the Non-Segmented model, Routing Algorithms for the Segmented Model.
Unit 2: Physical Design Automation of MCMs
Introduction to MCM Technologies, MCM Physical Design Cycle.

Module 5:
Unit 1: Chip Input and Output Circuits
ESD Protection, Input Circuits, Output Circuits and noise, On-chip clock Generation and Distribution, Latch-up and its prevention.

Textbooks:
1. Algorithms for VLSI Physical Design Automation by Naveed Shervani, 3rd Edition, 2005, Springer International Edition.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd ed., 2011.

Reference Books:
1. VLSI Physical Design Automation-Theory and Practice by Sadiq M Sait, Habib, Youssef, World Scientific.
2. Algorithms for VLSI Design Automation, S. H. Gerez, 1999, Wiley student Edition, John Wiley and Sons (Asia) Pvt. Ltd.
3. VLSI Physical Design Automation by Sung Kyu Lim, Springer International Edition.

E-Resources:

1. CAD innovation over the years (Short Video) https://www.youtube.com/watch?v=ZqQD95NhbXk.
2. Freeware and open source • 123D • LibreCAD • FreeCAD • BRL-CAD • OpenSCAD • NanoCAD • QCad • CAD Kernels • Parasolid by Siemens • ACIS by Spatial • Shape Manager by Autodesk • Open CASCADE • C3D by C3D Labs.
3. EDA: Where Electronic Begins (Short Video) https://www.youtube.com/watch?v=8uj81PWHlmk.
4. Zoom In to a Microchip (Short Video) https://www.youtube.com/watch?v=Fxv3JoS1uY8.
5. Intel: The Making of a Chip with 22nm/3D (Video) https://www.youtube.com/watch?v=d9SWNLZvA8g.
6. Low, K. (2016, April 20). A Look at Samsung Foundry's Business Strategy, Manufacturing Excellence and Advanced Technology Updates. Retrieved from https://www.samsungsemiblog.com/foundry/a-look-at-samsung-foundrys-business-strategy-manufacturing-excellence-and-advanced-technology-updates/.

Course Outcomes:

After completion of the course, students will be able to

1. establish comprehensive understanding of the various phases of CAD for Digital Electronic Systems, from digital logic simulation to physical design, including test and verification.
2. demonstrate knowledge and understanding of fundamental concepts in CAD and to establish capability for CAD tool development and enhancement.
3. practice the application of fundamentals of VLSI technologies.
4. optimize the implemented design for area, timing, and power by applying suitable constraints.
5. gain knowledge on the methodologies involved in design, verification, and implementation of digital designs on reconfigurable hardware platform (FPGA).

Course Code: LM63C	ARTIFICIAL INTELLIGENCE (Program Elective-V)	L	T	P	D
Credits: 3		3	0	0	0

Pre-requisite: Calculus, Linear algebra and Statistics.

Course Objectives:

1. To cater the knowledge of Neural Networks and Fuzzy Logic Control and use these for controlling real time systems.
2. To know about feedback networks.
3. To learn about the concept of fuzziness involved in various systems.
4. To understand the concept of adequate knowledge about fuzzy set theory.
5. To learn about comprehensive knowledge of fuzzy logic control and adaptive fuzzy logic and to design the fuzzy control using genetic algorithm.

Module 1:

Unit 1: Introduction

What is AI? Foundations of AI, History of AI, Agents and environments, The nature of the Environment.

Unit 2: Problem Solving

Problem solving Agents, Problem Formulation, Search Strategies.

Module 2:

Unit 1: Supervised Learning: Regression/Classification

Basic methods: Distance-based methods, Nearest-Neighbours, Decision Trees, Naive Bayes.

Unit 2: Linear models

Linear Regression, Logistic Regression, Generalized Linear Models Support Vector Machines, Nonlinearity and Kernel Methods.

Beyond Binary Classification: Multi-class/Structured Outputs, Ranking.

Module 3:

Unit 1: Unsupervised Learning Clustering

K-means/Kernel K-means.

Unit 2: Dimensionality Reduction

PCA and kernel PCA Matrix Factorization and Matrix Completion Generative Models (mixture models and latent factor models).

Module 4:

Unit 1: Biological foundations to intelligent Systems

Artificial Neural Networks. Single layer and Multilayer Feed Forward NN, LMS and Back Propagation.

Unit 2: Networks

Algorithm, Feedback networks and Radial Basis Function Networks.

Module 5:

Unit 1: Fuzzy Logic

Fuzzy Logic, Knowledge Representation, and Inference Mechanism.

Unit 2: Methods and Network

Defuzzification Methods Fuzzy Neural Networks and some algorithms to learn the parameters of the network like GA.

Textbooks:

1.Stuart Russell, Peter Norvig: "Artificial Intelligence: A Modern Approach",2nd Edition, Pearson Education, 2007.

2. Kevin Murphy, Machine Learning: A Probabilistic Perspective, MIT Press, 2012.

3.Trevor Hastie, Robert Tibshirani, Jerome Friedman, The Elements of Statistical Learning, Springer 2009 (freely available online).

4.Christopher Bishop, Pattern Recognition and Machine Learning, Springer, 2007.

5.J M Zurada , "An Introduction to ANN", Jaico Publishing House.

6.Simon Haykins, "Neural Networks", Prentice Hall.

Reference Books:

1. Artificial Neural Networks B. Yagna Narayana, PHI.
2. Artificial Intelligence, 2nd Edition, E.Rich and K.Knight (TMH).
3. Artificial Intelligence and Expert Systems – Patterson PHI.
4.Expert Systems: Principles and Programming- Fourth Edn, Giarrantana/ Riley,Thomson.
5. Neural Networks Simon Haykin PHI.

E- Resources:

1. Department of Computer Science, University of California, Berkeley, http://www.youtube.com/playlist?list=PLD52D2B739E4D1C5F
2. NPTEL: Artificial Intelligence, https://nptel.ac.in/courses/106105077/

Course Outcomes:

After completion of the course, students will be able to

1. develop an understanding of where and how AI can be used.
2. expose the students to the concepts of feed forward neural networks.
3. provide adequate knowledge about feedback networks.
4. understand the concept of fuzziness involved in various systems.
5. provide adequate knowledge about fuzzy set theory.