JBIET Academic Regulations - R25

Applicable to

Master of Technology (M. Tech)

Regular Two-Year Degree Programme
(For the Batches admitted from the Academic Year 2025-26)

J.B. INSTITUTE OF ENGINEERING AND TECHNOLOGY
(UGC AUTONOMOUS)
Bhaskar Nagar, Yenkapally (V), Moinabad (M), Hyderabad – 500075,
Telangana, India

AY 2025-26 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD

JBIET Academic Regulations - R25 Applicable to
M. Tech Regular Two-Year Degree Program
(For the Batches admitted from the Academic Year 2025- 26)
COURSE STRUCTURE AND SYLLABUS

I Year I Semester						
S.NO	**Code**	**Title of the Course**	**L**	**T**	**P**	**Credits**
1	NM61A	CMOS Digital IC Design	3	0	0	3
2	NM61B	CMOS Analog IC Design	3	0	0	3
3	NM61C NM61D NM61E	Device Modelling Embedded Real Time Operating Systems Nanomaterials and Nanotechnology	3	0	0	3
4	NM61F NM61G NM61H	Machine Learning and Deep Learning VLSI Architectures for Digital Signal Processing Scripting Languages for Design Automation	3	0	0	3
5	NM611	CMOS Digital IC Design Laboratory	0	0	4	2
6	NM612	CMOS Analog IC Design Laboratory	0	0	4	2
7	NME1A	Research Methodology & IPR	2	0	0	2
8		Audit Course–I	2	0	0	0
		Total Credits	**16**	**0**	**8**	**18**

		I Year II Semester				
S.NO	**Code**	**Title of the Course**	**L**	**T**	**P**	**Credits**
1	NM62A	Mixed Signal IC Design	3	0	0	3
2	NM62B	FPGA Based System Design	3	0	0	3
3	NM62C NM62D NM62E	VLSI Test and Testability Physical Design Automation with AI Functional Verification using System Verilog and UVM	3	0	0	3
4	NM62F NM62G NM62H	Low Power VLSI Design Microchip Fabrication Techniques Power Management IC Design	3	0	0	3
5	NM621	Mixed Signal IC Design Laboratory	0	0	4	2
6	NM622	FPGA Based System Design Laboratory	0	0	4	2
7	NM623	Mini Project with Seminar	0	0	4	2
8		Audit Course-II	2	0	0	0
		Total Credits	**14**	**0**	**12**	**18**

II Year I Semester						
S.NO	**Code**	**Title of the Course**	**L**	**T**	**P**	**Credits**
1	NM63A NM63B NM63C	CMOS RF IC Design Hardware Security in VLSI Design Advanced Memory Design and Architectures	3	0	0	3
2		Open Elective	3	0	0	3
3	NM631	Dissertation Work Review–II	0	0	18	6
		Total Credits	**6**	**0**	**18**	**12**

II Year II Semester						
S.NO	**Code**	**Title of the Course**	**L**	**T**	**P**	**Credits**
1	NM641	Dissertation Work Review-III	0	0	18	06
2	NM642	Dissertation Viva-Voce	0	0	42	14
		Total Credits	**0**	**0**	**60**	**20**

Open Electives						
S. No	**Code**	**Course Title**	**L**	**T**	**P**	**Credits**
1.	NMEO1	Business Analytics	3	0	0	3
2.	NM1OC	Industrial Safety	3	0	0	3
3.	NMEO3	Operations Research	3	0	0	3
4.	NMEO4	Cost Management of Engineering Projects	3	0	0	3
5.	NM3OD	Composite Materials	3	0	0	3

Audit Courses
English for Research Paper Writing Disaster Management
Sanskrit for Technical Knowledge Value Education
Constitution of India Pedagogy Studies
Stress Management by Yoga Personality Development through Life Enlightenment Skills

AY 2025-26 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD I Year – I Sem			
Course Code: NM61A	CMOS Digital IC Design	L	T	P	C
		3	0	0	3

Course Overview

This course introduces students to the foundational and advanced concepts in CMOS (Complementary Metal-Oxide-Semiconductor) digital integrated circuit design. Students will explore the principles, performance metrics, and design strategies for static and dynamic CMOS inverters, combinational and sequential logic gates, and complex digital systems. Emphasis is placed on understanding trade-offs in performance, power, area, and reliability in the context of technology scaling. The course also addresses interconnect modelling and modern layout methodologies, equipping students with practical and theoretical tools for custom and semi-custom digital IC design.

Course Outcomes (COs)

By the end of the course, students will be able to:

1. Analyze static and dynamic behavior of CMOS inverters using key performance metrics.
2. Design combinational logic circuits using static and dynamic CMOS styles.
3. Implement various sequential logic elements and pipelining techniques.
4. Apply custom and semi-custom design methodologies for digital ICs.
5. Evaluate interconnect effects and apply techniques to reduce parasitic impact.

Syllabus

Unit I: The CMOS Inverter

Introduction, the static CMOS inverter, Evaluating the robustness of the CMOS inverter – static behavior, Performance of CMOS inverter – dynamic behavior, Power, energy and energy-delay, Technology scaling and its impact on the inverter metrics.

Unit II: Designing Combinational Logic Gates in CMOS:

Introduction, Static CMOS design – complementary CMOS, ratioed logic, pass-transistor logic, Dynamic CMOS design – basic principles, speed and power dissipation of dynamic logic, Issues in dynamic design, cascading dynamic gates, Choosing a logic style, Designing logic for reduced supply voltage.

Unit III: Designing Sequential Logic Circuits:

Introduction – timing metrics for sequential circuits, Classification of memory elements, Static latches and registers – bistability principle, multiplexer-based latches, master-slave edge-triggered register, Low-voltage static latches, static SR flip-flops, Dynamic latches and registers – transmission gate edge-triggered registers, C2MOS, TSPCR, Pipelining – latch vs. register-based pipelines, NORA-CMOS

Unit IV: Implementation Strategies for Digital ICs:

Introduction, from custom to semi-custom and structured array design approaches, Custom circuit design, Cell-based design methodology, Array- based implementation approaches.

Unit V: Coping with Interconnect:

Introduction, Capacitive parasitics, Resistive parasitics, Inductive parasitics, Advanced interconnect techniques.

Text Book

1. Rabaey, Jan M., Anantha Chandrakasan, and Borivoje Nikolic. *Digital Integrated Circuits: A Design Perspective*. 2nd ed., Pearson Education, 2003.

Reference Books

1. Kang, Sung-Mo (Steve), and Yusuf Leblebici. *CMOS Digital Integrated Circuits: Analysis and Design*. 3rd ed., McGraw-Hill, 2003.
2. Uyemura, John P. *Introduction to VLSI Circuits and Systems*. Wiley, 2002.

Weste, Neil H.E., and David Harris. *CMOS VLSI Design: A Circuits and Systems Perspective*. 4th ed., Pearson Education, 2011.

AY 2025-26 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD I Year – I Sem			
Course Code: NM61B	CMOS Analog IC Design	L	T	P	C
		3	0	0	3

Course Overview

This course provides a comprehensive foundation in CMOS Analog Integrated Circuit Design, focusing on the analysis and design of key analog building blocks used in modern VLSI systems. It covers essential topics such as MOS device physics, single-stage and differential amplifiers, current mirrors, and operational amplifiers. Emphasis is placed on understanding the small-signal behavior, frequency response, and performance trade-offs in analog circuits. Students will gain skills in applying transistor-level models, analyzing analog circuit topologies, and designing biasing schemes, enabling them to develop robust analog IC solutions for real-world applications in consumer electronics, communications, and sensor interfaces.

Course Outcomes (COs)

By the end of this course, students will be able to:

1. Apply MOS device characteristics and second-order effects to analog circuit analysis.
2. Design single-stage MOS amplifier configurations for specific gain and impedance requirements.
3. Analyze the performance of differential amplifiers under common-mode and differential-mode operation.
4. Apply current mirror topologies to design biasing circuits in CMOS analog design.
5. Compare operational amplifier topologies considering gain, bandwidth, and power trade-offs.

Syllabus

Unit I: MOS Device Physics and Models:

Introduction to analog design, MOS device physics – General Considerations, MOS I/V Characteristics, Second-Order Effects, MOS Device Models.

Unit II: Single Stage Amplifiers:

Basic Concepts, Common-Source Stage with resistive-load and diode- connected load, Source Follower, Common-Gate Stage.

Unit III: Differential Amplifiers:

Single-Ended and Differential Operation, Basic Differential Pair, Common-Mode Response, Differential Mode with MOS Loads, Gilbert Cell.

Unit-IV: Passive and Active Current Mirrors:

Basic Current Mirrors, Cascade Current Mirrors, Active Current Mirrors

Unit-V: Operational Amplifiers:

General Considerations, One-Stage Op Amps, Two-Stage Op Amps, Gain Boosting, Comparison.

Textbook

1. Razavi, Behzad. *Design of Analog CMOS Integrated Circuits*. McGraw-Hill Education, 2001.

Reference Books

1. Allen, Philip E., and Douglas R. Holberg. *CMOS Analog Circuit Design*. 3rd ed., Oxford University Press, 2011.
2. Johns, David A., and Ken Martin. *Analog Integrated Circuit Design*. Wiley India, 2015.
3. Sansen, Willy M.C. *Analog Design Essentials*. Springer, 2006.

AY 2025-26 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD I Year – I Sem			
Course Code: NM61C	**Device Modeling(PE-I)**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

Course Overview:

This course focuses on the theoretical foundations and practical techniques for modeling MOSFET devices in the context of VLSI circuit design. It provides an in-depth understanding of semiconductor device physics, MOS capacitor behavior, MOSFET current-voltage characteristics, and advanced modeling concepts including capacitance, reliability, and parameter extraction. The course also covers how these models are integrated into simulation tools such as SPICE, enabling accurate performance prediction in modern IC design.

Course Outcomes (COs):

By the end of this course, students will be able to:

1. Explain the physical structure and electrical behavior of MOSFET devices.
2. Analyze and model MOS capacitors and threshold voltage characteristics.
3. Develop current-voltage and capacitance models for MOSFETs.
4. Evaluate device reliability issues and implement SPICE-based models.
5. Apply parameter extraction techniques and statistical modeling in circuit simulation.

Syllabus

Unit I: Fundamentals of MOSFET Structure and Device Physics:

Review of semiconductor physics and p–n junction, MOS transistor structure and operation, Scaling effects and parasitics, Modern VLSI device structures

Unit-II: MOS Capacitor and Threshold Voltage Modeling:

MOS capacitor - physics and C–V characteristics, Threshold voltage modeling: uniform and no uniform doping, Short-channel effects: DIBL, narrow-width effect, Temperature dependence of threshold voltage

Unit-III:

DC and Dynamic Modeling of MOSFETs: Charge-sheet and Pao–Sah current models, Subthreshold conduction and mobility degradation, Temperature effects on current characteristics, Capacitance models: Meyer model, charge-based model, Small-signal modeling

Unit-IV:

Reliability Modeling and SPICE Device Models: Hot-carrier degradation and reliability concerns, Gate and substrate currents, SPICE MOSFET models: LEVEL 1, 2, 3, Parameter definitions and usage in simulation

Unit-V:

Parameter Extraction and Statistical Modeling: Measurement techniques: C–V, threshold voltage, mobility, Parameter extraction using optimization techniques, Statistical modeling for process variation, Worst-case modeling in VLSI design

Textbooks

1. Arora, Narain. *MOSFET Modeling for VLSI Simulation: Theory and Practice*. Springer Science & Business Media, 2007.

Reference Books

1. Tsividis, Yannis, and Colin McAndrew. *Operation and Modeling of the MOS Transistor*. 3rd ed., Oxford University Press, 2011.
2. Sze, S. M., and Kwok K. Ng. *Physics of Semiconductor Devices*. 3rd ed., Wiley, 2006.
3. Trivedi, Subarna S., and Saurabh Kumar Gupta. *Semiconductor Device Modeling and Technology*. PHI Learning, 2012.
4. Muller, Richard S., and Theodore I. Kamins. *Device Electronics for Integrated Circuits*. 3rd ed., Wiley, 2002.

AY 2025-26 Onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD I Year – I Sem			
Course Code: NM61D	Embedded Real Time Operating System(PE-I)	L	T	P	C
		3	0	0	3

Course Overview

This course provides a comprehensive introduction to Real-Time Operating Systems (RTOS) and their applications in embedded systems. Students will explore the fundamental concepts of real-time embedded systems, understand task management, synchronization mechanisms like semaphores and message queues, and delve into exception handling and timer services. The course also covers memory management strategies and practical techniques for modularizing applications to meet real- time constraints. Additionally, it addresses common design challenges such as deadlocks and priority inversion, preparing students to design, analyses, and implement robust real-time embedded applications.

Course Outcomes (COs)

By the end of this course, students will be able to:

1. Analyze key concepts and roles of real-time operating systems in embedded system design.
2. Evaluate task scheduling and synchronization methods in real-time systems.
3. Design interrupt and timer handling mechanisms for embedded real-time environments.
4. Apply real-time memory management techniques in embedded applications.
5. Create modular real-time applications to resolve deadlocks and priority inversion.

Syllabus

Unit-I:

Introduction to RTOS: Real life examples of embedded systems, real-time embedded systems, the future of embedded systems, a brief history of operating systems, defining an RTOS, the scheduler, objects, services, key characteristics of an RTOS.

Unit-II:

Tasks: Introduction, defining a task, task states and scheduling, typical task operations, typical task structure, synchronization, communication, and concurrency.

Semaphores: Introduction, defining semaphores, typical semaphore operations, typical semaphore use.

Message Queues: Introduction, defining message queues, message queue states, message queue content, message queue storage, typical message queue operations, and typical message queue use. **Unit-III:**

Exceptions and Interrupts: Introduction, what are exceptions and interrupts, a closer look at exceptions and interrupts, processing general exceptions, the nature of spurious interrupts.

Timer and Timer Services: Introduction, real-time clocks and system clocks, programmable interval timers, timer interrupt service routines, a model for implementing the soft-timer handling facility, timing wheels, soft timers and timer related operations.

Unit-IV:

Memory Management: Introduction, dynamic memory allocation in embedded systems, fixed-size memory management in embedded systems, blocking vs. non-blocking memory functions, hardware memory management units.

Unit-V:

Modularizing Applications: Introduction, an outside-in approach to decomposing applications, guidelines and recommendations for identifying concurrency, schedulability analysis – rate monotonic analysis.

Common Design Problems: Introduction, resource classification, deadlocks, priority inversion.

Text Book

1. Qing Li, and Caroline Yao. *Real-Time Concepts for Embedded Systems*. CMP Books, 2003.

Reference Books

1. Prasad, K. V. K. K. *Embedded Real-Time Systems: Concepts, Design & Programming*. Dream Tech Press, 2005.
2. Simon, David E. *An Embedded Software Primer*. 1st ed., 5th impression, Addison-Wesley Professional, 2007.
3. Singh, Rajib Mall. *Real-Time Systems: Theory and Practice*. Pearson Education India, 2006.

AY 2025-26 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD I Year – I Sem			
Course Code: NM61E	Nanomaterials and Nanotechnology(PE-I)	L	T	P	C
		3	0	0	3

Course Overview

This course explores the fundamentals and advanced concepts of nanomaterials and nanotechnologies. It covers the unique physical and chemical properties of nanostructures across different dimensions (0D, 1D, 2D, and 3D), their synthesis methods, and applications. Students will learn about the size-dependent effects on material properties, nanolithography techniques, and the integration of nanomaterials in devices like MEMS and Nano electronics. Special emphasis is placed on carbon nanotubes (CNTs), ferroelectric materials, and emerging applications in biology, environment, and electronics.

Course Outcomes (COs)

By the end of this course, students will be able to:

1. Describe the fundamental properties and classification of nanomaterials across different dimensions.
2. Explain the various synthesis methods for nanostructures and their suitability for scaling applications.
3. Illustrate the working principles and fabrication processes of MEMS and nanolithography techniques.
4. Analyze the growth mechanisms, properties, and applications of carbon nanotubes (CNTs).
5. Evaluate the emerging applications of advanced nanomaterials in electronics, biology, and environmental fields.

Syllabus

Unit-I: Introduction to Nanomaterials and Nanotechnologies:

Features of nanostructures, Applications of nanomaterials and technologies, Nano-dimensional materials 0D, 1D, 2D structures, Size effects, Fraction of surface atoms, Specific surface energy, Surface stress, Effect on the lattice parameter, Phonon density of states, General methods for synthesis of nanostructures, Precipitative methods, Reactive methods, Hydrothermal/solvothermal methods, Suitability of synthesis methods for scaling, Potential uses.

Unit-II: Fundamentals and Classification of Nanomaterials:

Classification of nanomaterials, Zero- dimensional nanomaterials, One-dimensional nanomaterials, Two-dimensional nanomaterials, Three-dimensional nanomaterials, Low-dimensional nanomaterials and applications, Synthesis, properties and applications of low-dimensional carbon-related nanomaterials.

Unit-III:

Micro- and Nanolithography Techniques and MEMS: Micro- and nanolithography techniques, Emerging applications, Introduction to MEMS, Advantages and challenges of MEMS, Fabrication technologies, Surface micromachining, Bulk micromachining, Molding, Introduction to nano- photonics.

Unit-IV:

Carbon Nanotubes (CNTs): Introduction to CNTs, Synthesis of CNTs (arc-discharge, laser-ablation, catalytic growth), Growth mechanisms of CNTs, Multi-walled nanotubes, Single-walled nanotubes, Optical properties of CNTs, Electrical transport in perfect nanotubes, Applications of CNTs.

Unit-V:

Advanced Nanomaterials and Applications: Ferroelectric materials, Coating, Molecular electronics, Nano electronics, Biological and environmental applications, Membrane-based applications, Polymer-based applications.

Text Book

1. I. Gusev and A. A. Rempel. *Nanocrystalline Materials*. Cambridge International Science Publishing; 1st Indian edition, Viva Books Pvt. Ltd., 2008.
2. B. S. Murty, P. Shankar, Baldev Raj, B. B. Rath, and James Murday. *Nanoscience and Nanotechnology*. Tata McGraw-Hill Education, 2012.

Reference Books

1. Kenneth J. Klabunde and Ryan M. Richards, editors. *Nanoscale Materials in Chemistry*. 2nd ed., John Wiley & Sons, 2009.
2. Bharat Bhushan. *Springer Handbook of Nanotechnology*. 3rd ed., Springer, 2010.
3. Kamal K. Kar. *Carbon Nanotubes: Synthesis, Characterization and Applications*. 1st ed., Research Publishing Services, 2011.

AY 2025-26 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD I Year – I Sem			
Course Code: NM61F	Machine Learning and Deep Learning(PE-II)	L	T	P	C
		3	0	0	3

Course Overview

This course introduces the principles and practices of **Machine Learning and Deep Learning**, focusing on both theoretical understanding and practical implementation. It begins with the fundamentals of machine learning, including learning paradigms, model evaluation, and the challenges that have led to deep learning advances. The course then explores deep neural architectures, including feedforward networks, convolutional and recurrent networks, alongside critical concepts such as regularization and optimization. Finally, students are equipped with practical methodologies for building robust models and exposed to real-world applications across computer vision, speech recognition, and natural language processing.

Course Outcomes (COs)

By the end of this course, students will be able to:

1. Analyze machine learning algorithms and evaluate model performance using concepts like overfitting, bias-variance, and likelihood-based estimation.
2. Design deep feedforward neural networks using appropriate architectures, activation functions, and backpropagation techniques.
3. Apply regularization and optimization techniques to improve generalization and training efficiency of deep neural networks.
4. Implement convolutional and recurrent neural network models for processing spatial and sequential data.
5. Evaluate model performance and deployment strategies in real-world applications such as computer vision, NLP, and speech recognition.

Syllabus

Unit-I: Machine Learning Basics:

Learning algorithms, Capacity, overfitting and under fitting, estimators, bias and variance, maximum likelihood estimation, Bayesian statistics, Supervised and unsupervised learning algorithms, building a machine learning algorithm, challenges motivating deep learning.

Unit-II: Deep Feedforward Networks:

Gradient-based learning, hidden units, architecture design, back- propagation and other differentiation algorithms.

Unit-III: Regularization for Deep Learning:

Norm penalties, Dataset augmentation, multi-task learning, early stopping, sparse representations, ensemble methods, dropout. **Optimization:** Optimization for Training Deep Models, challenges in neural network optimization, basic algorithms, parameter initialization strategies, algorithms with adaptive learning rates.

Unit-IV: Convolutional Neural Networks:

The convolution operation, motivation, pooling, convolution and pooling as an infinitely strong prior, variants of the basic convolution function, structures outputs,

Data types, efficient convolution algorithms, random or unsupervised features.

Sequence Modeling:
Recurrent and Recursive Nets, Recurrent Neural Networks, Recursive Neural Networks, Long Short-Term Memory, optimization for long-term dependencies.

Unit-V: Practical Methodology:
Performance metrics, selecting hyper parameters, debugging strategies. **Applications:** Large-scale deep learning, computer vision, speech recognition, natural language processing, other applications.

Text Book

1. Good fellow, Ian, Yoshua Bengio, and Aaron Courville. *Deep Learning*. MIT Press, 2016.

Reference Books

1. Géron, Aurélien. *Hands-On Machine Learning with Scikit-Learn, Keras, and TensorFlow*. 2nd ed., O'Reilly Media, 2019.
2. Bishop, Christopher M. *Pattern Recognition and Machine Learning*. Springer, 2006.
3. Chollet, François. *Deep Learning with Python*. 2nd ed., Manning Publications, 2021.

AY 2025-26 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD I Year – I Sem			
Course Code: NM61G	VLSI Architectures for Digital Signal Processing(PE-II)	L	T	P	C
		3	0	0	3

Course Overview

This course provides a comprehensive study of Very Large Scale Integration (VLSI) architectures tailored for Digital Signal Processing (DSP) systems. It explores the principles, techniques, and hardware implementations that support high-performance DSP applications in modern CMOS technologies. Topics include algorithmic representations, iteration bounds, pipelining, parallelism, unfolding, folding, and convolution techniques, as well as bit-level and redundant arithmetic architectures. The course also introduces the design and use of programmable DSP processors, with a focus on real-time, low-power, and high-throughput design requirements.

Course Outcomes (COs)

By the end of this course, students will be able to:

1. Identify typical DSP algorithms and analyze their computational requirements for efficient VLSI implementation.
2. Compute iteration bounds and apply retiming techniques to optimize DSP data flow graphs for performance.
3. Design pipelined and parallel FIR filters and utilize unfolding and folding methods for architectural transformations.
4. Implement fast convolution methods and develop efficient bit-level and redundant arithmetic units for DSP systems.
5. Evaluate and compare programmable DSP processor architectures for various application domains such as mobile and multimedia systems

Syllabus

Unit I: Introduction to Digital Signal Processing Systems:

Introduction, typical DSP algorithms, DSP application demands and scaled CMOS technologies. **Iteration Bound:** data-flow graph representations, loop bound, and iteration bound, algorithms for computing iteration bound. **Pipelining and Parallel Processing:** Introduction, pipelining of FIR digital filters, parallel processing. **Retiming:** Definitions and properties, solving systems of inequalities, retiming techniques.

Unit II: Unfolding:

An algorithm for unfolding, properties and applications of unfolding. **Folding:** Folding transformation, register minimization techniques, folding of multirate systems

Unit III: Fast Convolution

Introduction, Cook-Toom algorithm, Winograd algorithm, iterated convolution, cyclic convolution, design of fast convolution algorithm by inspection.

Unit IV: Bit-Level Arithmetic Architectures

Introduction, parallel multipliers, bit-serial multipliers, bit- serial filter design and implementation. **Redundant Arithmetic:** Introduction, redundant number representations, carry-free radix-2 addition and subtraction, radix-2 hybrid redundant multiplication architectures, data format conversion, redundance to nonredundant converter.

Unit V: Programmable Digital Signal Processors:

Introduction, evolution of programmable digital signal processors, important features of DSP processors, DSP processors for mobile and wireless communications, processors for multimedia signal processing.

Text Book

1. Parhi, Keshab K. *VLSI Digital Signal Processing Systems: Design and Implementation*. Wiley, 1999.

Reference Books

1. V. K. Madisetti, *VLSI Digital Signal Processors: An Introduction to Rapid Prototyping and Design Synthesis*, IEEE Press, New York.
2. Meyer-Baese, Uwe. *Digital Signal Processing with Field Programmable Gate Arrays*. 4th ed., Springer, 2014.
3. S. Y. Kung, H. J. Whitehouse, *VLSI and Modern Signal Processing*, Prentice Hall.

AY 2025-26 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD I Year – I Sem			
Course Code: NM61H	Scripting Languages for Design Automation(PE-II)	L	T	P	C
		3	0	0	3

Course Overview

This course introduces the use of scripting languages—PERL, TCL, and Python—in the context of Electronic Design Automation (EDA) workflows. Students will learn to write efficient automation scripts for parsing tool outputs, managing design files, and controlling EDA tools such as synthesis and simulation environments. The course emphasizes practical application, covering syntax, control structures, file I/O, regular expressions, and data processing. By the end of the course, learners will be able to automate common VLSI design tasks, improve productivity, and select the appropriate scripting language based on the use case.

Course Outcomes (COs)

By the end of this course, students will be able to:

1. Describe the role of scripting languages in EDA workflows and differentiate between scripting and compiled languages.
2. Write PERL scripts to perform text parsing, data extraction, and report generation.
3. Develop TCL scripts to automate tool commands and control design processes in EDA tools.
4. Construct Python scripts for file handling, data processing, and automation of design-related tasks.
5. Compare the features of PERL, TCL, and Python, and select suitable scripting languages for specific EDA applications.

Syllabus

Unit I:

Introduction to Scripting Languages in EDA: Introduction to scripting and automation, Scripting vs compiled languages, Using interpreters and writing first scripts in Perl, Tcl, and Python, Command-line execution, Variable types and assignments (overview), Control flow basics (if, loops – overview), Basic file I/O (overview), Importance of scripting in EDA tools and flows.

Unit II:

PERL Scripting: Scalar data, Arrays and list data, Hashes, Input and output, Control structures, Regular expressions, Pattern matching with regex, Substitution and translation, Using files and file handles, String manipulation, Subroutines, Using Perl modules, Command-line arguments and environment variables, Text parsing examples, Report generation

Unit III: TCL Scripting:

Tcl syntax and structure, Variables and data types, Lists and arrays, Expressions and operators, Control flow (if, switch, while, for, for each), Procedures and variable scope, File input and output, String and list manipulation, Error handling, Working with commands and arguments, Tool-specific scripting conventions, Example tool scripts for synthesis and simulation

Unit IV: Python for Design Automation and Data Processing:

Python basics and data types, Expressions and operators, Flow control (if, for, while), Functions, Lists and dictionaries, String manipulation, File reading and writing, Pattern matching with regular expressions, Working with CSV and JSON files, Automating the keyboard and mouse, Using os, sys, and subprocess modules, Writing utility scripts for automation

Unit V: Advanced Integration and Comparison:

Comparison of PERL, TCL, and Python features, Strengths and weaknesses in EDA use-cases, Best practices for automation and maintainability, Calling external commands and shell integration in all three languages, Script interoperability using intermediate files (CSV, JSON), Efficiency, readability, and debugging considerations, Choosing the right scripting language for given EDA tasks

Text Books

1. Schwartz, Randal L., brian d foy, and Tom Phoenix. *Learning Perl*. 7th ed., O'Reilly Media, 2016.
2. Welch, Brent B., Ken Jones, and Jeffrey Hobbs. *Practical Programming in Tcl and Tk*. 4th ed., Prentice Hall, 2003.
3. Sweigart, Al. *Automate the Boring Stuff with Python: Practical Programming for Total Beginners*. 2nd ed., No Starch Press, 2019.

Reference Books

1. Robbins, Arnold. *Scripting the UNIX System: Using Bash, Perl, and More*. Addison-Wesley, 2003.
2. Ousterhout, John K. *Tcl and the Tk Toolkit*. 2nd ed., Addison-Wesley Professional, 2009.
3. Python Software Foundation. *Python Language Reference Manual*. https://docs.python.org.

AY 2025-26 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD I Year – I Sem			
Course Code: NM611	CMOS Digital IC Design Laboratory	L	T	P	C
		0	0	4	2

Course Overview

This course provides a comprehensive introduction to CMOS digital circuit design, focusing on the fundamental building blocks such as inverters, combinational and sequential logic circuits, and their implementation strategies. Students will explore device physics, design techniques, timing analysis, and the impact of interconnect parasitics on circuit performance. Through practical experiments, learners gain hands-on experience in designing, simulating, and analyzing CMOS circuits, preparing them for advanced work in VLSI and digital IC design.

Course Outcomes (COs)

By the end of this course, students will be able to:

1. Design and analyze the static and dynamic behavior of CMOS inverters.
2. Implement and simulate basic CMOS combinational logic gates using various design styles.
3. Develop and verify sequential logic circuits such as latches and flip-flops.
4. Compare different CMOS design methodologies including custom, semi-custom, and array- based approaches.
5. Evaluate the impact of interconnect parasitics on the performance and reliability of CMOS circuits.

List of Experiments (Minimum 12 Experiments)

1. **Measure Voltage Transfer Characteristic (VTC) of CMOS Inverter:**Design a static CMOS inverter and plot the input vs. output voltage to determine switching threshold and noise margins.
2. **Determine Propagation Delay of CMOS Inverter:**Apply a square wave input, simulate the output waveform, and measure the rise time, fall time, and propagation delay.
3. **Design and Simulate CMOS NAND Gate:**Implement a 2-input NAND gate using CMOS and verify its truth table and transient response.
4. **Compare Static CMOS and Pass-Transistor NAND Gate:**Design both logic styles for NAND gate, simulate output voltage levels, and compare delay and power.
5. **Design a Dynamic CMOS NOR Gate:**Create a dynamic NOR gate, simulate precharge and evaluation phases, and observe output waveform timing.
6. **Implement and Simulate a Static SR Latch:**Design an SR latch using CMOS transistors; verify bistability by applying input set/reset sequences.
7. **Design a Master-Slave D Flip-Flop:**Build a master-slave edge-triggered flip-flop, apply clock and data inputs, and verify timing and output behavior.
8. **Compare Latch-Based and Register-Based Pipeline Stages:**Design a simple 2-stage pipeline using latches and registers; simulate and compare data propagation delays.

9. **Custom vs Standard Cell Design of a 2-Input AND Gate:** Implement a 2-input AND gate using full custom transistor-level design and standard cell approach; compare layout area.
10. **Array-Based Implementation of a 2-Bit Adder:** Design a 2-bit adder using an array-based logic style; simulate functional correctness and evaluate area.
11. **Analyze Delay Due to Capacitive Load on CMOS Inverter:** Add different load capacitances to inverter output and simulate the resulting delay variation.
12. **Effect of Interconnect Resistance on Signal Propagation:** Model a resistive interconnect connected to a CMOS inverter output; simulate delay and signal attenuation.
13. **Simulate Interconnect RC Parasitics Impact on Output Waveform:** Extract parasitic RC values for a simple wire segment and simulate their effect on signal rise and fall times.
14. **Compare Signal Integrity with and without Interconnect Inductance:** Model a simple interconnect with inductance; simulate signal ringing and delay effects compared to purely RC models.

AY 2025-26 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD I Year – I Sem			
Course Code: NM612	CMOS Analog IC Design Laboratory	L	T	P	C
		0	0	4	2

Course Overview

This laboratory course complements the theory of analog CMOS design by providing hands-on experience with MOS device characterization, amplifier circuits, differential pairs, current mirrors, and operational amplifiers. Students will learn to design, simulate, and analyze fundamental analog building blocks using industry-standard tools. The experiments emphasize understanding device physics, circuit behavior, and performance trade-offs in real-time conditions, preparing students for practical analog integrated circuit design.

Course Outcomes (COs)

After successful completion of this laboratory course, students will be able to:

1. Design and simulate MOS transistors to analyse their electrical characteristics and model parameters.
2. Implement and evaluate single-stage amplifiers including common-source, source follower, and common-gate configurations.
3. Design differential amplifiers with resistive and active loads and measure their gain and common-mode rejection properties.
4. Develop basic, cascade, and active current mirrors, analysing their current replication and output impedance.
5. Design and analyse two-stage CMOS operational amplifiers focusing on gain, stability, and frequency response.

List of Experiments (Minimum 12 Experiments)

1. **MOSFET I-V Characteristics Simulation:** Design and simulate NMOS and PMOS transistors to plot ID vs VDS and ID vs VGS characteristics; analyze threshold voltage and saturation behavior.
2. **Effect of Second-Order Parameters on MOS Device Performance:** Simulate and study effects like channel length modulation, body effect, and velocity saturation on transistor I-V characteristics.
3. **Extraction of MOS Device Model Parameters Using SPICE:** Extract and verify MOSFET parameters (threshold voltage, mobility, etc.) from device simulation for different model levels.
4. **Design and Simulation of Common-Source Amplifier with Resistive Load:** Design a common-source amplifier and analyze voltage gain, input/output impedance, and frequency response.
5. **Design and Simulation of Common-Source Amplifier with Diode-Connected Load:** Implement a CS amplifier with diode-connected load and compare gain and linearity with resistive-load version.
6. **Design and Analysis of Source Follower (Common-Drain) Amplifier:** Build a source follower circuit; simulate and measure voltage gain, output impedance, and linearity.

7. **Design and Simulation of Common-Gate Amplifier:** Design a common-gate stage and analyze its input/output characteristics and high-frequency response.
8. **Design of Basic Differential Pair with Resistive Load:** Simulate a differential pair and analyze differential gain, common-mode gain, and calculate CMRR.
9. **Differential Amplifier with MOS Current Mirror Load:** Implement a differential pair with active current mirror load; analyze improvements in gain and CMRR.
10. **Simulation of Gilbert Cell Mixer:** Design a Gilbert cell circuit and simulate frequency mixing operation with two sinusoidal inputs.
11. **Design and Simulation of Basic Current Mirror:** Implement a basic current mirror; simulate output current accuracy and dependence on transistor sizing.
12. **Design and Simulation of Cascade Current Mirror:** Build a cascade current mirror; analyze output impedance and current matching improvement.
13. **Design of Active Current Mirror Circuits:** Implement Wilson or improved current mirrors; simulate and compare performance with basic and cascade types.
14. **Design and Simulation of Two-Stage CMOS Operational Amplifier:** Design a two-stage op-amp; analyze gain, phase margin, unity gain bandwidth, and frequency response.

AY 2025-26 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD I Year – I Sem			
Course Code: NME1A	Research Methodology and IPR	L	T	P	C
		3	0	0	3

Course Overview:

This course is designed to introduce students to the fundamental aspects of research methodology and intellectual property rights (IPR). It focuses on identifying and defining research problems, conducting effective literature reviews, writing technical reports and research proposals, and understanding the ethical aspects of research. The course also provides in-depth knowledge of intellectual property laws, including patents, copyrights, trademarks, and geographical indications. Students will learn the process of patenting, the global IPR scenario, and the importance of protecting innovations in a knowledge-driven economy.

Course Outcomes (COs)

By the end of this course, students will be able to:

1. Formulate research problems by identifying research gaps, objectives, and scope.
2. Analyze literature and research data while ensuring ethical standards and avoiding plagiarism.
3. Develop well-structured technical reports and research proposals using appropriate academic formats.
4. Evaluate types of intellectual property to determine suitable protection strategies for innovations.
5. Apply intellectual property rights concepts to emerging fields such as biotechnology, software, and traditional knowledge.

Syllabus

Unit I:

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, Data collection, Analysis, Interpretation, Necessary instrumentations.

Unit II:

Effective literature studies approaches, Analysis, Plagiarism, Research ethics.

Unit III:

Effective technical writing, how to write a report, paper in developing a research proposal, Format of research proposal, A presentation and assessment by a review committee.

Unit IV:

Nature of Intellectual Property: Patents, Designs, Trade and Copyright.
Process of Patenting and Development: Technological research, Innovation, Patenting, Development. International Scenario: International cooperation on Intellectual Property, Procedure for grant of patents, Patenting under PCT.

Unit V:

Patent Rights: Scope of Patent Rights, Licensing and transfer of technology, Patent information and databases, Geographical Indications.

New Developments in IPR: Administration of Patent System, New developments in IPR, IPR of Biological Systems, Computer Software etc. Traditional knowledge, Case Studies, IPR and IITs.

Textbooks:

1. Melville, Stuart, and Wayne Goddard. *Research Methodology: An Introduction for Science & Engineering Students*.
2. Goddard, Wayne, and Stuart Melville. *Research Methodology: An Introduction*.

Reference Books:

1. Kumar, Ranjit. *Research Methodology: A Step-by-Step Guide for Beginners*. 2nd ed.
2. Halbert, Debora J. *Resisting Intellectual Property*. Taylor & Francis, 2007.
3. Mayall, W. H. *Industrial Design*. McGraw-Hill, 1992.
4. Niebel, Benjamin W. *Product Design*. McGraw-Hill, 1974.
5. Asimov, Morris. *Introduction to Design*. Prentice Hall, 1962.
6. Merges, Robert P., Peter S. Menell, and Mark A. Lemley. *Intellectual Property in the New Technological Age*. 2016.
7. Ramappa, T. *Intellectual Property Rights under WTO*. S. Chand, 2008

AY 2025-26 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD I Year – II Sem			
Course Code: NM62A	Mixed Signal IC Design	L	T	P	C
		3	0	0	3

Course Overview

This course provides a solid foundation in the analysis and design of mixed-signal integrated circuits (ICs), which combine analog and digital functionality on a single chip. It emphasizes signal theory, sampling methods, analog and digital filter design, and the architecture and analysis of data converters. Students will learn the fundamental concepts, mathematical tools, and circuit techniques needed to design real-world mixed-signal systems, with applications in communications, data acquisition, and signal processing.

Course Outcomes (COs)

By the end of this course, students will be able to:

1. Analyze sinusoidal signals and frequency-domain representations using Fourier tools and z- transform methods.
2. Evaluate the effects of sampling, aliasing, and interpolation on analog signals and implement sample-and- hold circuits.
3. Design analog filters using active-RC, MOSFET-C, and gm-C topologies and interpret discrete-time filtering behavior.
4. Implement basic digital filters using FIR/IIR techniques and evaluate performance using DAC/ADC SPICE models.
5. Assess the performance of data converters based on quantization noise, SNR, and apply noise- shaping methods to improve resolution.

Syllabus

Unit I: Signals, Filters and Tools:

Sinusoidal signals, in-phase and quadrature signals, the complex (z-) plane, comb filters – the digital comb filter, the digital differentiator, the digital integrator, representing signals – exponential Fourier series, Fourier transform, Dirac Delta function.

Unit II: Signals, Filters and Tools:

Sampling – impulse sampling, decimation, the sample-and-hold (S/H), S/H spectral response, the reconstruction filter (RCF), circuit concerns for implementing the S/H, interpolation, Zero padding, Hold register, linear interpolation, K-path sampling – switched-capacitor circuits, non-overlapping clock generation, implementing the S/H, the S/H with gain.

Unit III: Analog Filters:

Integrator building blocks – low pass filters, active-RC integrators, MOSFET-C integrators, gm- C (transconductance-C) integrators, discrete-time integrators, filtering topologies – the bilinear transfer function, the bquadratic transfer function

Unit IV: Digital Filters

– SPICE models for DACs and ADCs, the ideal DAC, the ideal ADC, Sinc-shaped digital filters, band pass and high pass Sinc filters, interpolation using Sinc filters, filtering topologies – FIR filters, the bilinear transfer function, the bilinear transfer function.

Unit V: Data Converters:

Quantization noise, signal-to-noise ratio (SNR), clock jitter, improving SNR using averaging, the one-bit ADC and DAC, passive noise-shaping, improving SNR and linearity.

Text Books

1. R. Jacob Baker, *CMOS Mixed-Signal Circuit Design*, Second Edition, Wiley–IEEE Press, 2008.

Reference Books

1. Razavi, Behzad. *Design of Analog CMOS Integrated Circuits*. 2nd ed., McGraw-Hill Education, 2017.
2. Johns, David A., and Ken Martin. *Analog Integrated Circuit Design*. Wiley, 1997.
3. Sansen, Willy M.C. *Analog Design Essentials*. Springer, 2006.
4. Allen, Phillip E., and Douglas R. Holberg. *CMOS Analog Circuit Design*. 2nd ed., Oxford University Press, 2002.

AY 2025-26 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD I Year – II Sem			
Course Code: NM62B	FPGA Based System Design	L	T	P	C
		3	0	0	3

Course Overview

This course introduces the principles and practices of FPGA-based system design, with a strong focus on digital logic implementation, system architecture, and modern design methodologies. Students will gain hands-on experience with hardware description languages, combinational and sequential logic design, and explore advanced topics such as platform FPGAs and multi-FPGA systems. The course equips learners with foundational knowledge and practical skills to architect, design, and optimize embedded digital systems using FPGAs. Suitable for postgraduate students in electronics, embedded systems, or VLSI design, this course bridges the gap between traditional digital logic design and modern reconfigurable computing.

Course Outcomes (COs)

By the end of this course, students will be able to:

1. Explain the architectural features and functional components of FPGA-based systems and describe their advantages in digital design applications.
2. Design combinational logic circuits using Verilog HDL and evaluate them for delay, power, and resource utilization on FPGA platforms.
3. Develop and simulate sequential logic circuits and finite state machines using appropriate design styles and clocking rules.
4. Apply behavioral design methodologies and demonstrate system modeling using HDLs in real-world case studies.
5. Analyze and propose solutions for large-scale FPGA-based systems involving busses, platform FPGAs, and multi-FPGA architectures.

Syllabus

Unit I: Introduction to FPGA-Based Systems:

Introduction, basic concepts, digital design and FPGAs, FPGA-based system design, FPGA architectures, SRAM-based FPGAs, permanently programmed FPGAs, chip I/O, circuit design of FPGA fabrics, and architecture of FPGA fabrics.

Unit II: Combinational Logic Design in FPGAs

: Introduction, the logic design process, hardware description languages
-modeling with HDLs, Verilog, Combinational network delay, power and energy optimization, arithmetic logic, logic implementation for FPGAs, physical design for FPGAs, the logic design process revisited

Unit III: Sequential Logic and State Machines:

Introduction, the sequential machine design process, sequential design styles, rules for clocking, performance analysis, and power optimization

Unit IV: Design Methodologies and Behavioral Architecture:

Introduction, behavioral design, design methodologies, design example

Unit V: System-Level Design and Advanced FPGA Applications:

Introduction, buses, platform FPGAs, multi-FPGA systems, Novel architectures

Text Books

1. Wolf, Wayne. *FPGA-Based System Design*. Pearson Education India, 2005.

Reference Books

1. Maxfield, Clive. *The Design Warrior's Guide to FPGAs: Devices, Tools and Flows*. Newnes, 1st ed., 2004.
2. Trimberger, Stephen M. *Field-Programmable Gate Array Technology*. Springer Science & Business Media, 2012.
3. Kuon, Ian, Russell Tessier, and Jonathan Rose. *FPGA Architecture: Survey and Challenges*. Now Publishers Inc., 2007.

AY 2025-26 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD I Year – I I Sem			
Course Code: NM62C	VLSI Test and Testability(PE-III)	L	T	P	C
		3	0	0	3

Course Overview

This course introduces students to digital system testing techniques and fault diagnosis in VLSI circuits. It covers fault models, test generation methods for combinational and sequential circuits, and various design-for-testability (DFT) strategies. Students will explore scan-based designs, Built- In Self-Test (BIST) techniques, memory testing algorithms, and fault diagnosis methods. Emphasis is placed on practical testing challenges in digital and embedded systems to ensure reliability and fault tolerance.

Course Outcomes (COs)

By the end of this course, students will be able to:

1. Identify different types of faults in digital circuits and explain their corresponding logical fault models.
2. Apply test generation techniques to detect faults in combinational and sequential digital circuits.
3. Design scan-based and ad-hoc DFT architectures for improving circuit testability.
4. Implement Built-In Self-Test (BIST) strategies for digital systems and memory blocks.
5. Analyze fault diagnosis techniques to locate and interpret faults in logic-level digital circuits.

Syllabus

Unit-I: Basics of Testing and Fault Modeling: Introduction

To Testing - Faults in digital circuits - Modeling of faults - Logical Fault Models - Fault detection - Fault location - Fault dominance - Logic Simulation - Types of simulation
- Delay models - Gate level Event-driven simulation.

Unit-II: Test Generation for Combinational and Sequential Circuits:

Test generation for combinational logic circuits - Testable combinational logic circuit design - Test generation for sequential circuits - design of testable sequential circuits. Design for Testability

Unit-III: Design for Testability:

Ad-hoc design - Generic scan-based design - Classical scan-based design – System level DFT approaches.

Unit-IV: Self-Test and Test Algorithms:

Built-In Self-Test - Test pattern generation for BIST - Circular BIST - BIST Architectures - Testable Memory Design - Test algorithms - Test generation for Embedded RAMs.

Unit-V: Fault Diagnosis:

Logic Level Diagnosis - Diagnosis by UUT reduction - Fault Diagnosis for Combinational Circuits - Self-checking

Text Books

1. Abramovici, M., M. A. Breuer, and A. D. Friedman. *Digital Systems Testing and Testable Design*. 1st ed., Jaico Publishing House, 2002.
2. Bushnell, M. L., and V. D. Agrawal. *Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits*. Illustrated ed., Springer Science & Business Media, 2006

Reference Books

1. Lala, P. K. *Digital Circuit Testing and Testability*. Academic Press, 2002.

2. Crouch, A. L. *Design-for-Test for Digital IC's and Embedded Core Systems*. 1st ed., Prentice Hall International, 1999

AY 2025-26 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD I Year – II Sem			
Course Code: NM62D	Physical Design Automation with AI(PE-III)	L	T	P	C
		3	0	0	3

Course Overview

This course introduces students to the fundamentals of VLSI physical design and explores how Artificial Intelligence (AI) is transforming Electronic Design Automation (EDA). Students will gain a comprehensive understanding of the VLSI design flow, physical design stages, partitioning algorithms, placement, routing, clock tree synthesis, and timing closure. The course also introduces the role of machine learning in optimizing physical design processes, covering key applications and challenges. Emphasis is placed on design rules, optimization techniques, and algorithmic approaches essential for real-world chip design.

Course Outcomes (COs)

By the end of this course, students will be able to:

1. Explain the physical design flow in VLSI and apply basic graph algorithms used in EDA tools.
2. Demonstrate understanding of chip planning techniques including floor planning, placement, and routing.
3. Analyze and implement routing strategies and clock tree synthesis for efficient signal distribution.
4. Evaluate timing closure techniques to ensure performance and reliability in VLSI designs.
5. Identify and discuss the applications and limitations of machine learning in physical design automation.

Syllabus

Unit-I: Introduction to Physical Design and AI in EDA:

Introduction - Electronic Design Automation (EDA), VLSI Design Flow, VLSI Design Styles, Layout Layers and Design Rules, Physical Design optimizations, Algorithms and Complexity, Graph Theory Terminology, Common EDA Terminology. Netlist and System Partitioning– Introduction, KL and FM Algorithms, Multilevel Partitioning.

Unit-II: Chip Planning and Placement:

Introduction, optimization goals, floorplan representations, floor planning algorithms, pin assignment, power and ground routing. Global placement, legalization and detailed placement.

Unit-III: Routing and Clock Tree Synthesis:

Introduction, optimization goals, representations of routing regions, the global routing flow, single-net and full-net routing, detailed routing – horizontal and vertical constraint graphs, channel and switchbox routing, area routing, clock routing, modern clock tree synthesis.

Unit – IV: Timing Closure:

Timing analysis, and performance constraints, timing-driven placement, timing- driven routing, physical synthesis, performance-driven design flow.

Unit-V: Machine Learning in Physical Design:

Introduction ML promises and challenges in physical design, Canonical ML applications, the state of ML for physical design.

Text Book

1. Kahng, Andrew B., et al. *VLSI Physical Design: From Graph Partitioning to Timing Closure*. 2nd ed., Springer International Publishing, 2022.
2. Sherwani, Naveed A. *Algorithms for VLSI Physical Design Automation*. 3rd ed., Springer, 2012

Reference Books

1. Hsiao, Michael. *Machine Learning Applications in Electronic Design Automation*. Morgan & Claypool, 2020.
2. Cong, Jason, and Bei Yu. *Machine Learning and AI for EDA: From Fundamentals to Advanced Applications*. Springer, 2022.

AY 2025-26 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD I Year – II Sem			
Course Code: NM62E	Functional Verification using System Verilog and UVM(PE-III)	L	T	P	C
		3	0	0	3

Course Overview

This course provides a comprehensive introduction to functional verification using System Verilog and the Universal Verification Methodology (UVM). Starting with foundational System Verilog language constructs and object-oriented programming, the course gradually introduces advanced verification concepts including randomization, coverage, and inter-process communication. Building on this foundation, students learn the UVM framework for creating reusable and scalable test benches, focusing on UVM components, sequences, transactions, and transaction-level modeling (TLM). Hands-on exercises and real-world examples solidify understanding, preparing students for practical verification challenges in ASIC and FPGA design environments.

Course Outcomes (COs)

By the end of this course, students will be able to:

1. Write basic System Verilog test benches using data types, control statements, and functions.
2. Use object-oriented programming and randomization to create flexible and reusable test benches.
3. Measure verification quality using functional coverage in System Verilog.
4. Build UVM test benches using components like tests, drivers, monitors, and agents.
5. Use UVM sequences and communication ports to send transactions and collect results.

Syllabus

Unit I: System Verilog Fundamentals:

Verification Guidelines – Introduction, verification process, basic test bench functionality, test bench components, simulation environment phases, and test bench performance. Data Types – built- in data types, arrays, linked lists, creating new types and user- defined structures, constants, strings. Procedural Statements and Routines – tasks, functions, and void functions, routine arguments, returning from a routine. Local data storage, time values.

Unit II: Test bench and OOP Concepts:

Connecting the Test bench and Design–separating the test bench and design, the interface construct, stimulus timing, interface driving and sampling, connecting it all together, program-module interactions, System Verilog assertions. Basic OOP – define a class, creating new objects, object deallocation, class routines, dynamic objects, copying objects, building a test bench. Randomization – Introduction, randomization in System Verilog, constraint details, solution probabilities, valid and in-line constraints, iterative and array constraints, random control, random generators, random device configuration.

Unit-III: Advanced Concepts for UVM Readiness:

Threads and Interprocess Communication – working with threads, interprocess communication, events, semaphores, mailboxes, building testbench with threads and IPC. Advanced OOP and Testbench Guidelines – inheritance, factory patterns, type casting and virtual methods, composition, inheritance, and alternatives, copying an object, callbacks. Functional Coverage – coverage types, strategies, anatomy of a cover group, triggering, data sampling, cross coverage.

Unit-IV: UVM Infrastructure:

Introduction, UVM Components, UVM Tests, UVM Transactions, UVM Sequences

Unit-V: UVM Integration & TLM (Transaction-Level Modeling) Communication

UVM Agents, Using Analysis Ports in a Testbench, Put and Get Ports in Action, UVM Reporting.

Text Book

1. Spear, Chris. *System Verilog for Verification: A Guide to Learning the Testbench Language Features*. 2nd ed., Springer, 2014.
2. Salemi, Ray. *UVM Primer: A Step-by-Step Introduction to the Universal Verification Methodology*. Mentor Graphics, 2014.

Reference Books

1. Mathur, Ashok B. *Advanced Functional Verification: Concepts and Techniques*. Springer, 2021.
2. Bhasker, J., and Rakesh Chadha. *System Verilog for Verification: A Guide to Learning the Testbench Language Features*. Prentice Hall, 2007.
3. Bergeron, Janick. *System Verilog for Verification: A Guide to Learning the Testbench Language Features*. 3rd ed., Springer, 2012.

AY 2025-26 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD I Year – II Sem			
Course Code: NM62F	Low Power VLSI Design(PE-IV)	L	T	P	C
		3	0	0	3

Course Overview

This course focuses on the principles and techniques for designing energy-efficient CMOS VLSI circuits. Students will learn about the sources and modeling of power dissipation in modern integrated circuits, and methods for estimating and optimizing power consumption at various design levels. Topics include low-power design strategies at the device, circuit, logic, architecture, and software levels. The course also explores emerging techniques like adiabatic computing, pass- transistor logic, and asynchronous circuit design for ultra-low-power applications.

Course Outcomes (COs)

By the end of this course, students will be able to:

1. Identify sources of power dissipation in CMOS circuits and explain methods to reduce them.
2. Apply power estimation techniques to evaluate energy usage in combinational and sequential logic circuits.
3. Use architectural and circuit-level transformations to optimize designs for low power consumption.
4. Design and test low-voltage CMOS circuits considering submicron effects and leakage currents.
5. Explore and apply advanced low-power techniques such as adiabatic logic and software-level power optimization.

Syllabus

Unit I: Low-Power CMOS VLSI Design:

Introduction, Sources of Power Dissipation, Designing for Low Power. Physics of Power Dissipation in CMOS FET Devices- MIS structure, Long Channel and Sub-micron MOSFET, Gate Induced Drain Leakage, Power dissipation in CMOS-Short Circuit and Dynamic Dissipation, Load Capacitance.

Unit II: Power Estimation in CMOS Circuits:

Modelling of signals, Signal Probability Calculation, Probabilistic Techniques for Signal Activity Estimation. Statistical Techniques -Estimating Average Power in Combinational and Sequential Circuits, Estimation of Glitching Power, Power Estimation using Input Vector Compaction, Power Dissipation in DominoCMOS.

Unit III: Synthesis for Low Power:

Behavioural Level Transforms - Algorithm Level Transforms,Power Constrained Least Squares Optimization for Adaptive and Non-adaptive Filters, Circuit Activity Driven Architectural Transformations, Architecture Driven Voltage Scaling,Power Optimization using Operation Reduction and Substitution, Precomputation-Based Optimization for Low Power, Logic and Circuit Level Optimization for Low Power.

Unit IV: Design and Test of Low Voltage CMOS Circuits:

Introduction, Circuit Design Styles, Leakage Current in Deep Sub-micrometer Transistors, Deep Sub-micrometer Device Design Issues, Minimizing Short Channel Effect, Low Voltage Circuit Design Techniques – ReverseVgs, Steeper Subthreshold Swing, Multiple Threshold Voltages, Multiple Supply Voltages.

Unit V: Advanced Techniques:

Adiabatic Computation, Pass Transistor Logic Synthesis, Asynchronous Circuits. Software Design for Low Power: Introduction, Sources of Software Power Dissipation, Software Power Estimation and Optimization.

Text Book

1. Roy, Kaushik, and Carat C. Prasad. *Low-Power CMOS VLSI Circuit Design*. Wiley-IEEE Press, 2000.
2. Rabaey, Jan M., Anantha Chandrakasan, and Borivoje Nikolic. *Digital Integrated Circuits: A Design Perspective*. 2nd ed., Prentice Hall, 2003.

Reference Books

1. Chandrakasan, Anantha P., and Robert W. Brodersen. *Low Power Digital CMOS Design*. Kluwer Academic Publishers, 1995.
2. Pedram, Massoud. *Power-Aware Design Methodologies*. Springer, 2005.

AY 2025-26 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD I Year – II Sem			
Course Code: NM62G	Microchip Fabrication Techniques(PE-IV)	L	T	P	C
		3	0	0	3

Course Overview

This course provides a comprehensive introduction to the principles and processes involved in semiconductor fabrication, focusing on silicon-based microchip manufacturing. Students will explore the semiconductor industry, material properties, and crystal growth techniques essential for wafer preparation. The course covers wafer fabrication methods, contamination control, and yield optimization. Key lithography and patterning techniques, including advanced photolithography, doping, and thin-film deposition, are studied in detail. Finally, metallization, device evaluation, packaging, and the business aspects of wafer fabrication complete the curriculum, preparing students for roles in VLSI fabrication and semiconductor manufacturing industries.

Course Outcomes:

By the end of this course, students will be able to:

1. Describe the semiconductor industry landscape and explain the properties of semiconductor materials and wafer preparation techniques.
2. Outline the wafer fabrication process and apply contamination control and productivity improvement methods.
3. Demonstrate understanding of lithography and patterning processes used in semiconductor manufacturing.
4. Explain advanced lithography techniques, doping processes, and thin-film deposition methods for device fabrication.
5. Analyze metallization techniques, device evaluation procedures, packaging methods, and the business considerations of wafer fabrication.

Syllabus

Unit-I: Semiconductor Industry and Materials:

The Semiconductor Industry, Properties of Semiconductor Materials and Chemicals, Crystal Growth and Silicon Wafer Preparation

Unit-II: Wafer Fabrication and Contamination Control:

Overview of Wafer Fabrication, Contamination Control, Productivity and Process Yields, Oxidation

Unit-III: Lithography Processes – Patterning Steps:

The Ten-Step Patterning Process — Surface Preparation to Exposure, the Ten-Step Patterning Process — Developing to Final Inspection

Unit-IV:

Advanced Lithography, Doping, and Deposition: Advanced Photolithography Processes, Doping, Layer Deposition

Unit-V: Metallization, Device Evaluation, Business, and Packaging:

Metallization, Process and Device Evaluation, The Business of Wafer Fabrication, Introduction to Devices and Integrated Circuit Formation, Introduction to Integrated Circuits, Packaging

Text Books

1. Van Zant, Peter. *Microchip Fabrication: A Practical Guide to Semiconductor Processing*. 6th ed., McGraw- Hill, 2014.

Reference Books

1. Ghandhi, Sorab K. *VLSI Fabrication Principles: Silicon and Gallium Arsenide*. 2nd ed., Wiley, 1994.
2. Sze, Simon M., and Kwok K. Ng. *Physics of Semiconductor Devices*. 3rd ed., Wiley-Interscience, 2006.
3. Streetman, Ben G., and Sanjay Banerjee. *Solid State Electronic Devices*. 7th ed., Pearson, 2014.
4. Wolf, Stephen, and Richard N. Tauber. *Silicon Processing for the VLSI Era*. Vol. 1, Lattice Press, 1986.

AY 2025-26 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD I Year – II Sem			
Course Code: NM62H	Power Management IC Design(PE-IV)	L	T	P	C
		3	0	0	3

Course Overview

This course provides a comprehensive understanding of modern Power Management Integrated Circuits (PMICs), emphasizing the principles, design methodologies, and implementation challenges across various topologies such as linear regulators, inductive converters, and switched- capacitor converters. Through theoretical analysis and practical case studies (e.g., smartphones and IoT), students will develop skills to design energy-efficient, high- performance power management solutions suited for SoCs and complex embedded systems. The course also includes peripheral circuit design for sensing, protection, and control integration.

Course Outcomes (COs)

By the end of this course, students will be able to:

1. Describe the roles, architectures, and functional requirements of Power Management ICs (PMICs) and their application in modern electronic systems.
2. Design linear voltage regulators, including advanced and digital LDOs, considering efficiency, stability, and transient performance.
3. Analyze inductive DC-DC converter topologies (buck, boost, buck-boost, multi-phase, SIMO) with emphasis on performance metrics and control techniques.
4. Implement switched capacitor and charge pump converters for integrated, compact, and efficient power management solutions.
5. Integrate gate driver circuits, protection mechanisms, and sensing modules to ensure reliability and safety in PMICs.

Syllabus:

Unit-I: Fundamentals of Power Management ICs:

Role and requirements of Power Management ICs (PMICs), the smartphone as a typical example, fundamental concepts - linear regulator, the inductive DC-DC converter, the Switched capacitor converters, the hybrid converter, power delivery - lateral and vertical, integrated voltage regulator (IVR), dynamic voltage and frequency scaling (DVFS).

Unit-II: Linear Voltage Regulators:

Fundamental circuit and control concept, drop voltage and power efficiency, frequency behavior and stability, fast transient techniques and slew-rate enhancement, PSRR, output noise, soft- start, Advanced LDO types: capacitor-less, flipped voltage follower, Digital LDOs: ADC, digital controller, limit cycle oscillations.

Unit-III: Inductive DC-DC Converters:

The fundamental Buck converter, voltage conversion ratio, ripple, losses and power conversion efficiency, inductor and capacitor sizing, voltage-mode and current- mode control, Loop compensation: Type I, II, III compensators, Constant on-time and hysteretic control, DCM operation and burst mode, Boost, buck-boost, and flyback converters, Multi-phase converters: ripple cancellation, phase shedding, Single inductor multiple output (SIMO) converters.

Unit-IV: Switched-Capacitor (SC) and Charge Pump Converters:

Basic operation of charge pumps: diode-based and transistor-based, Parasitic effects, charge sharing, and efficiency, SC converter topologies: Dickson, ladder, Fibonacci, Charge flow modeling and output resistance, Gate drive techniques, Capacitor and switch sizing, multi-phase and multi-ratio SC converters, interleaving, ripple reduction, and closed-loop control.

Unit-V: Gate Drivers, Protection, and Sensing:

Gate driver architectures: CMOS inverters, cascaded drivers, Bootstrap techniques and dv/dt triggering, Level shifters: resistor-based, cross-coupled, capacitive, Current sensing methods: shunt, replica, DCR, Protection circuits: OVP, thermal shutdown, UVLO, power-on-reset, Bandgap reference circuits and trimming, Zero-cross detection and current limiting.

Text Books

1. Wicht, Bernhard. *Design of Power Management Integrated Circuits*. Wiley, 2024.

Reference Books

1. Erickson, Robert W., and Dragan Maksimovic. *Fundamentals of Power Electronics*. 2nd ed., Springer, 2001.
2. Basso, Christophe. *Switch-Mode Power Supplies: SPICE Simulations and Practical Designs*. McGraw-Hill Education, 2008.
3. Wu, Jinrong, and Ray Ridley. *Power Supply Design: A Practical Guide*. Springer, 2019.

AY 2025-26 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD I Year – I I Sem			
Course Code: NM621	Mixed Signal IC Design Laboratory	L	T	P	C
		0	0	4	2

Course Overview

This course introduces the fundamental concepts of signal processing and filter design, focusing on both analog and digital domains. Students will explore signal representation, sampling theory, aliasing, and various filtering techniques including analog integrators, digital filters, and data converters. The course combines theoretical knowledge with practical experiments to develop skills in designing, simulating, and analyzing signal processing circuits and systems.

Course Outcomes (COs)

By the end of this course, students will be able to:

1. Analyze and represent signals using sinusoidal components and the complex z-plane.
2. Design and evaluate sample-and-hold circuits and interpolation techniques to mitigate aliasing effects.
3. Implement and analyze analog filter circuits including active-RC, MOSFET-C, and gm-C integrators.
4. Design and simulate digital filters such as comb, Sinc-shaped, and FIR filters using bilinear transform methods.
5. Model and evaluate the performance of data converters including ideal DACs and ADCs.

List of Experiments (Minimum 12 Experiments)

1. **Sinusoidal Signals and Quadrature Components:** Generate and analyze sinusoidal signals including their in-phase and quadrature components to understand signal representation.
2. **Signal Representation on Complex (z-) Plane:** Plot signals on the complex z-plane and analyze their magnitude and phase characteristics.
3. **Digital Comb Filter Design:** Design and simulate a digital comb filter and analyze its frequency response to understand notch filtering.
4. **Digital Differentiator and Integrator:** Implement digital differentiator and integrator circuits and analyze their time and frequency domain responses.
5. **Impulse Sampling and Aliasing Analysis:** Simulate impulse sampling and study the aliasing effect in the frequency spectrum of the sampled signal.
6. **Sample-and-Hold (S/H) Circuit Analysis:** Design a sample-and-hold circuit and analyze its spectral response and effect on signal reconstruction.
7. **Interpolation Techniques:** Implement zero padding and linear interpolation methods on sampled data to improve signal resolution.
8. **Switched-Capacitor Sample-and-Hold Circuit:** Design a switched-capacitor sample-and-hold circuit with non-overlapping clocks and analyze its performance.

9. **Active-RC Low-Pass Integrator Design:** Design and simulate an active-RC low-pass integrator filter and analyze its frequency response.
10. **MOSFET-C and gm-C Integrator Design:** Implement MOSFET-C and gm-C integrators, compare their characteristics and frequency response.
11. **Discrete-Time Integrator Design:** Design and analyze discrete-time integrator circuits to understand their filtering behavior.
12. **Ideal DAC and ADC Modeling:** Model ideal DAC and ADC circuits, and analyze their input-output characteristics and linearity.
13. **Sinc-Shaped Digital Filter Design:** Design Sinc-shaped digital filters including band pass and high pass filters and analyze their frequency response.
14. **FIR Filter Implementation Using Bilinear Transfer Function:** Implement FIR filters using the bilinear transfer function and analyze filter characteristics like gain and phase response.

AY 2025-26 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD I Year – I I Sem			
Course Code: NM622	FPGA Based System Design Laboratory	L	T	P	C
		0	0	4	2

Course Overview

This laboratory course focuses on practical hands-on experience with FPGA design and implementation using Hardware Description Languages (HDLs) such as Verilog or VHDL. Students will learn to design, simulate, and implement fundamental digital building blocks, combinational and sequential circuits, and complex systems like finite state machines and communication modules on FPGA platforms. The course covers a range of topics from basic logic gates and arithmetic units to real-time systems and digital signal processing applications. Emphasis is placed on simulation, verification, and hardware validation to bridge the gap between theoretical concepts and real- world digital system design.

Course Outcomes (COs)

By the end of this course, students will be able to:

1. Write and simulate HDL code for basic combinational and sequential digital circuits using Verilog HDL.
2. Design and implement complex digital systems such as FSMs, arithmetic logic units, and communication modules on FPGA platforms.
3. Develop and verify interfacing protocols for external hardware devices like seven-segment displays, keypads, and UART communication.
4. Apply design methodologies for timing, synchronization, and resource optimization in FPGA-based digital system design.
5. Demonstrate the ability to deploy and debug digital designs on FPGA development boards, validating functionality through hardware testing

List of Experiments (Any 12 Experiments)

1. **LED Blinking Using Verilog:** Implement a basic LED blink circuit to understand FPGA programming and output pin control.
2. **Design and Simulation of Basic Logic Gates using Verilog HDL:** To write HDL code for basic logic gates (AND, OR, NOT, XOR), simulate their functionality, and verify the outputs using a waveform viewer.
3. **Implementation of 4-bit Adder/Subtractor on FPGA:** To design and implement a 4-bit adder/subtractor using Verilog, simulate and verify functionality on an FPGA development board.
4. **Design of a 4x1 Multiplexer and 1x4 Demultiplexer:** To write and simulate Verilog code for a 4x1 MUX and 1x4 DEMUX and validate outputs through FPGA implementation.
5. **Comparator Design (2-bit or 4-bit):** Design a simple digital comparator circuit that compares two binary inputs.
6. **Design and Implementation of a 4-bit Synchronous Counter:** To implement a 4-bit up/down synchronous counter using HDL, simulate for timing and logic correctness, and deploy it on FPGA hardware.
7. **Finite State Machine (FSM) Design:** Sequence Detector-To design a Moore or Mealy FSM for sequence detection, simulate the state transitions, and implement the design on an FPGA board.
8. **Design and Implementation of an ALU Supporting Basic Operations:** To design an Arithmetic Logic Unit that performs basic arithmetic and logic functions (ADD, SUB, AND, OR, NOT) and test it on FPGA.

9. **Interfacing Seven Segment Display with FPGA:** To write HDL code to drive a seven-segment display with binary or BCD inputs and implement the interface on FPGA hardware.
10. **Shift Register (Left/Right):** Design a shift register that shifts input bits left or right on each clock pulse.
11. **Implementation of Traffic Light Controller using FSM on FPGA:** To design a traffic light controller using finite state machines, simulate its time sequence, and implement it on FPGA hardware.
12. **PWM Signal Generation using FPGA:** To implement a pulse-width modulation (PWM) generator using Verilog HDL and demonstrate its use in applications like LED brightness control.
13. **Real-Time Clock Design and Display using FPGA:** To implement a real-time clock on FPGA with hour- minute-second display and use multiplexed seven-segment display for output.
14. **Serial Input with UART Receiver (Basic):** Implement a simple UART receiver to receive serial data and blink an LED.
15. **Implementing Digital Filters (FIR/IIR) on FPGA:** To implement a basic Finite Impulse Response (FIR) or Infinite Impulse Response (IIR) filter in HDL and simulate its output for given inputs.

AY 2025-26 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD II Year – I Sem			
Course Code: NM63A	CMOS RF IC Design(PE-V)	L	T	P	C
		3	0	0	3

Course Overview

This course introduces the principles and design methodologies of CMOS Radio Frequency Integrated Circuits (RFICs). Students will learn to design and analyse critical RF building blocks such as low-noise amplifiers (LNAs), mixers, oscillators, and phase-locked loops (PLLs) in CMOS technology. Emphasis is placed on RF system-level understanding, noise and nonlinearity modeling, frequency planning, matching networks, and CMOS implementation strategies. The course combines theory, design practice, and simulation insights essential for modern wireless and communication IC design.

Course Outcomes (COs)

By the end of this course, students will be able to:

1. Analyze RF system-level parameters such as gain, noise figure, and non-linearity using standard performance metrics.
2. Design CMOS small-signal amplifier circuits, including LNAs, with appropriate impedance matching and noise optimization techniques.
3. Implement CMOS oscillator circuits such as LC and ring oscillators with attention to phase noise and frequency stability.
4. Evaluate the performance of CMOS mixer circuits focusing on frequency conversion efficiency, linearity, and noise behaviour.
5. Apply the principles of PLLs and frequency synthesizers to develop CMOS-based frequency generation solutions for RF systems.

Syllabus

Unit I: Introduction to RF Design and CMOS Technology:

Review of RF system fundamentals - system gain, noise figure, nonlinearities, and link budget. Review of CMOS technology, basic MOSFET RF equivalent circuit model, advanced MOSFET RF equivalent circuit model, SPICE modeling of CMOS RF circuits – SPICE level 3 and BSIM parameters.

Unit II: Small-Signal MOS Amplifier for RF:

Basic amplifying structure, improvements to the basic amplifying structure, amplifier matching (LC and inductive), low-noise amplifiers (LNAs) – noise modeling for common source and common gate LNAs.

Unit III: CMOS Oscillator Circuits:

Review of general feedback principles, fixed-frequency oscillators, ring oscillator, voltage control of oscillators, oscillator phase noise and estimation.

Unit IV: CMOS Mixer Circuits:

General mixer concepts, single MOS mixer topologies, balanced MOSFET mixers, image rejection circuit topologies, I/Q mixer topologies.

Unit V: CMOS PLLs and Frequency Synthesizers:

Introduction to the phase lock loop – definitions and basic operation, phase detection and phase-frequency detection, loop filters, PLL noise behaviour, PLL behavioural modeling. Frequency Synthesis – PLL-based synthesizers, direct digital synthesis.

Text Book

1. Robert H. Caverly, *CMOS RFIC Design Principles*, Artech House, 2016.

Reference Books

1. Thomas H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge University Press, 2nd Edition.
2. Behzad Razavi, *RF Microelectronics*, Prentice Hall, 2nd Edition.
3. R. Jacob Baker, *CMOS: Circuit Design, Layout, and Simulation*, Wiley IEEE Press, 3rd Edition.
4. Ali M. Niknejad, *RF CMOS: Modeling and Technology for Wireless Design*, Cambridge University Press.
5. David M. Pozar, *Microwave Engineering*, Wiley, 4th Edition.

AY 2025-26 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD II Year – I Sem			
Course Code: NM63B	Hardware Security in VLSI Design(PE-V)	L	T	P	C
		3	0	0	3

Course Overview

This course provides an in-depth understanding of security challenges and vulnerabilities in modern VLSI systems, particularly within SoC and PCB designs. Students will learn about hardware threats such as Trojans, reverse engineering, IP piracy, side-channel attacks, test-oriented and physical attacks, and how to design secure hardware using primitives like PUFs and TRNGs. Through a mix of theoretical foundations and hands-on experimentation, students will be equipped to identify, analyse, and mitigate hardware security threats in real-world VLSI systems.

Course Outcomes (COs)

By the end of this course, students will be able to:

1. Identify and explain the key layers and components of VLSI systems vulnerable to hardware attacks.
2. Analyze different types of hardware Trojans and IP piracy techniques and suggest appropriate countermeasures.
3. Evaluate side-channel and test-oriented attacks on SoC and FPGA-based systems using suitable models.
4. Demonstrate an understanding of physical attacks and PCB vulnerabilities through attack modeling and analysis.
5. Design and implement hardware security primitives such as PUFs and TRNGs to protect VLSI designs from cloning and counterfeiting.

Syllabus

Unit I: Introduction to Hardware Security:

Overview of a computing system, layers of a computing system, hardware security vs. hardware trust, attacks, vulnerabilities and countermeasures, conflict between security and test/debug, evolution of hardware security, overview of electronic hardware – nanoscale technologies, ASICs and FPGAs, printed circuit board, embedded systems, hardware- firmware-software interaction.

Unit II: Hardware Trojans

Introduction, SoC design flow, hardware Trojans, hardware Trojans in FPGA designs, hardware Trojans taxonomy, trust benchmarks, countermeasures against hardware Trojans, and hardware Trojan attacks. **Hardware IP Piracy and Reverse Engineering:** Introduction, hardware intellectual property (IP), security issues in IP-based SoC design, security issues in FPGA, reverse engineering and tampering.

Unit III: Side-Channel Attacks:

Introduction, taxonomy of side-channel attacks, uncommon side-channel attacks, and power analysis attacks, electromagnetic (EM) side-channel attacks, fault-injection attacks, timing attacks. **Test-Oriented Attacks:** Introduction, scan-based attacks, JTAG-based attacks.

Unit IV: Physical Attacks and Countermeasures:

Introduction, reverse engineering, probing attack.

Attacks on PCB: Security challenges, attack models, bus snooping attack.

Unit-V: Hardware Security Primitives:

Introduction, physical unclonable functions (PUFs), true random number generator (TRNG), design of anti-counterfeit, existing challenges and attacks.

Security and Trust Assessment: Security assets and attack models, pre-silicon and post-silicon security and trust assessment.

Text Book

1. Bhunia, Swarup, and Mark M. Tehranipoor. *Hardware Security: A Hands-on Learning Approach*. 1st ed., Academic Press, 2019.

Reference Books

1. Tehranipoor, Mark, and Cliff Wang, editors. *Introduction to Hardware Security and Trust*. Springer, 2012.
2. Bhunia, Swarup, and Sandip Ray. *Fundamentals of IP and SoC Security: Design, Verification, and Debug*. Springer, 2017.
3. Wolf, Marilyn. *Embedded System Interfacing: Design for the Internet-of-Things (IoT)*. Morgan Kaufmann, 2019.
4. Skorobogatov, Sergei. *Semi-Invasive Attacks: A New Approach to Hardware Security Analysis*. Springer, 2007.

AY 2025-26 onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	M.Tech-VLSISD II Year – I Sem			
Course Code: NM63C	Advanced Memory Design and Architectures(PE-V)	L	T	P	C
		3	0	0	3

Course Overview

This course provides an in-depth exploration of memory systems and architectures in modern and next-generation computer systems. Starting from the foundational concepts of caching and memory hierarchy, the course advances through on-chip network design, multicore memory consistency, DRAM system architectures, and emerging non- volatile memory technologies. It emphasizes architectural modeling, performance optimization, and system-level design trade-offs relevant to current and future computing platforms, including those used in high-performance and embedded systems.

Course Outcomes (COs)

By the end of this course, students will be able to:

1. Describe the structure, operation, and performance aspects of cache memory systems, including advanced designs like trace caches and prefetching.
2. Analyze the architecture and performance of on-chip networks (NoCs), including routing mechanisms and router design.
3. Explain memory models, identify data races, and apply concepts like transactional memory in multicore systems.
4. Illustrate the organization and timing of DRAM systems and evaluate the role of memory controllers.
5. Compare various emerging memory technologies and recommend suitable types for specific system-level applications

Syllabus

Unit-I: Caches:

Memory hierarchy and the notion of caches, virtual memory, modeling and designing a cache, advanced cache design, trace caches, instruction prefetching, data prefetching.

Unit-II: The On-chip Network:

Overview of an NoC, message transmission, routing, design of a router, non-uniform cache architectures, performance aspects.

Unit-III: Multicore Systems:

Parallel programming, issues in parallel hardware, theoretical foundations of memory models, memory models, data races, transactional memory.

Unit-IV: DRAMs:

DRAM cell, capacitors used in DRAM cells, array of DRAM cells, a computer system with DRAM arrays, design spaces of DRAMs, DDR generations and timing, buffered DIMMs, DRAM access protocols, DRAM timing, memory controller.

Unit-V: Emerging Memory Technologies:

Flash memory, ferroelectric RAM (FeRAM), magneto resistive RAM (MRAM), phase change memory (PCM), resistive RAM (ReRAM), 3D and embedded memory technologies.

Text Book

Sarangi, Smruti R. *Next-Gen Computer Architecture: Till the End of Silicon*. Version 3.1, Smruti R. Sarangi, 2023.

Reference Books

1. Jacob, Bruce, Spencer W. Ng, and David T. Wang. *Memory Systems: Cache, DRAM, Disk*. Morgan Kaufmann, 2008.
2. Sharma, Ashok K. *Semiconductor Memories: Technology, Testing, and Reliability*. Wiley-IEEE Press, 1997.
3. Hennessy, John L., and David A. Patterson. *Computer Architecture: A Quantitative Approach*. 6th ed., Morgan Kaufmann, 2019.

Keeth, Brent, et al. *DRAM Circuit Design: Fundamental and High-Speed Topics*. Wiley-IEEE Press, 2007.